

GM5MPHY/GM7MxxP

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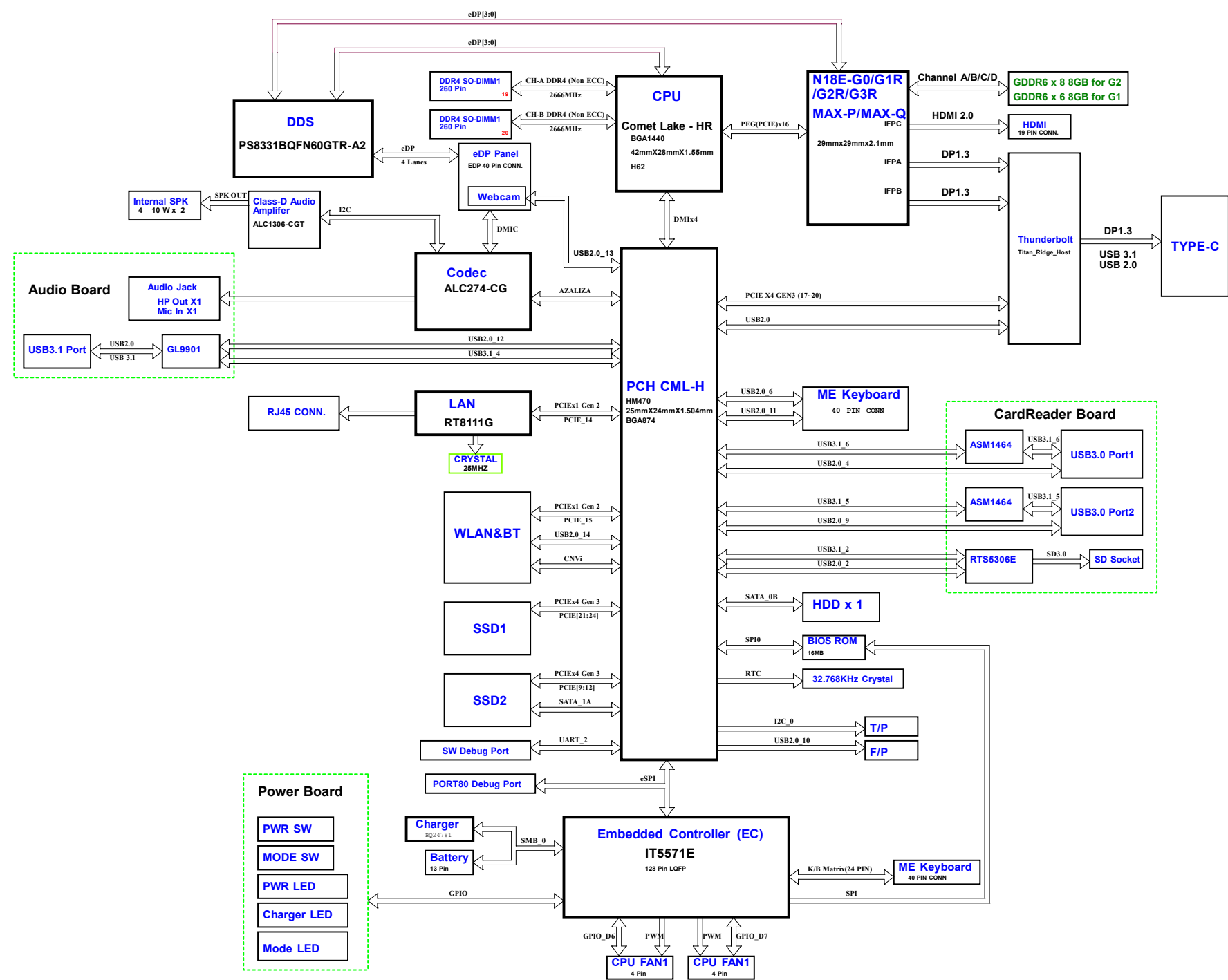
M/B Schematic Version Change List

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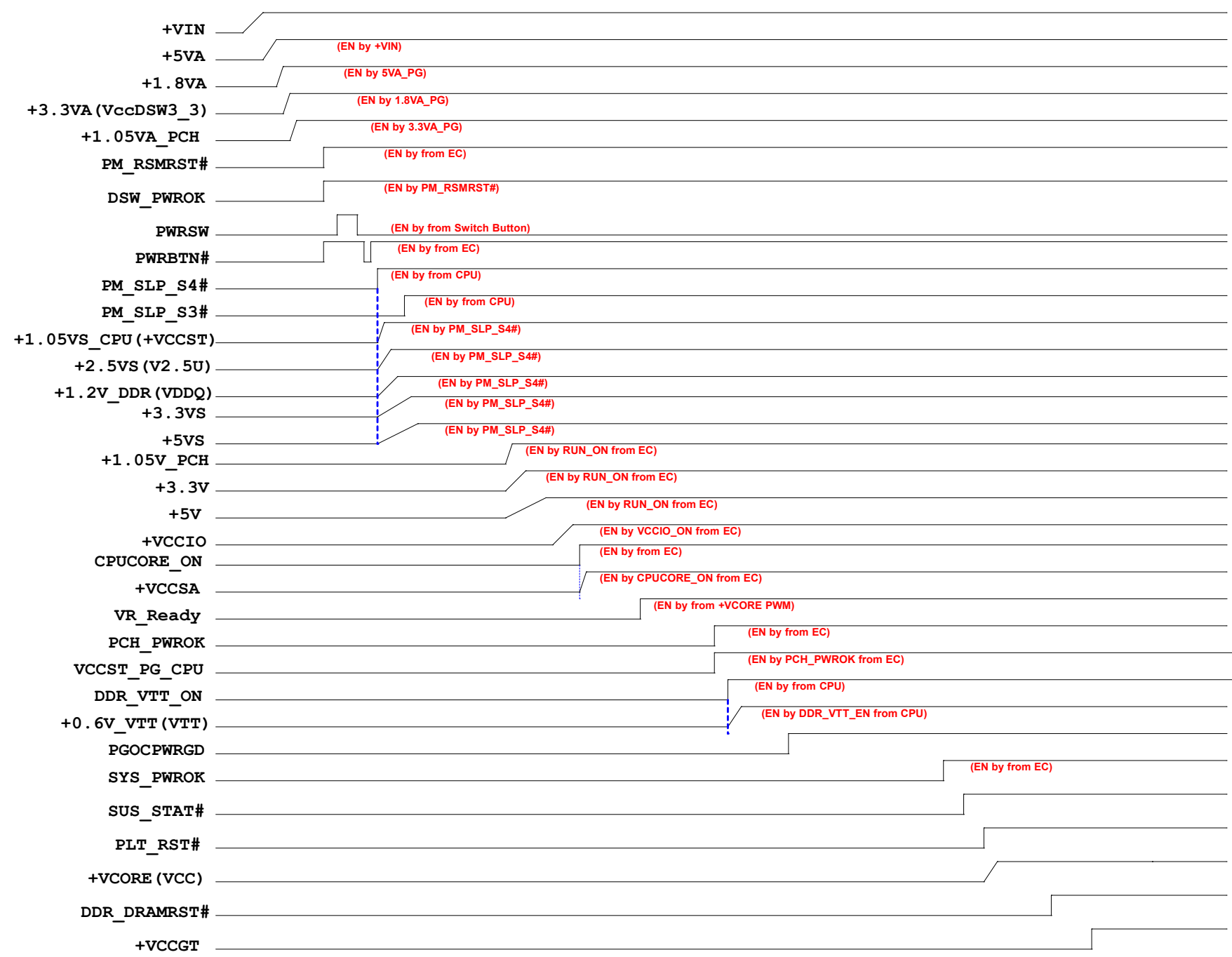
Daughter Board Schematic Version Change List

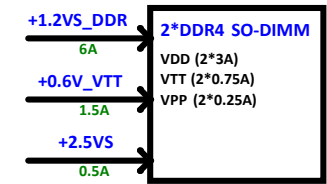
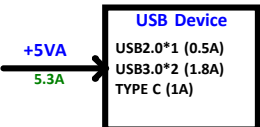
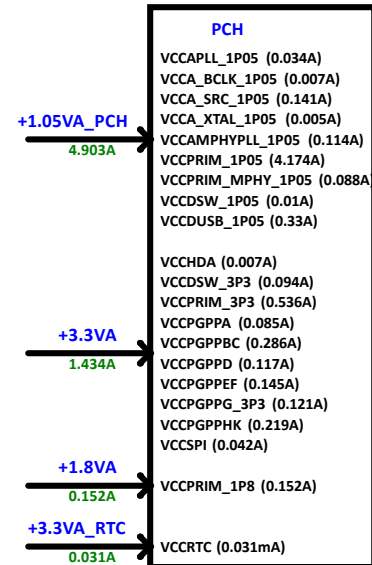
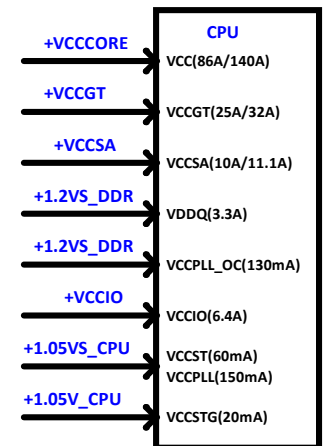
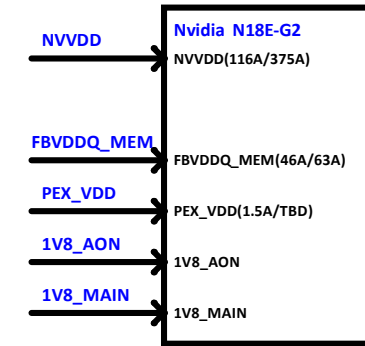
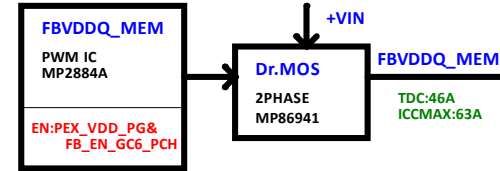
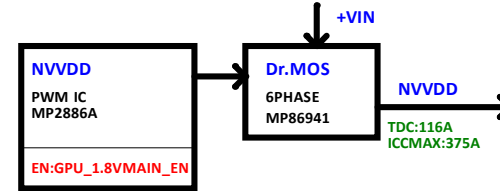
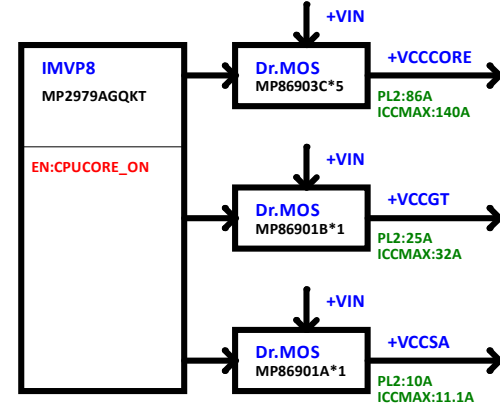
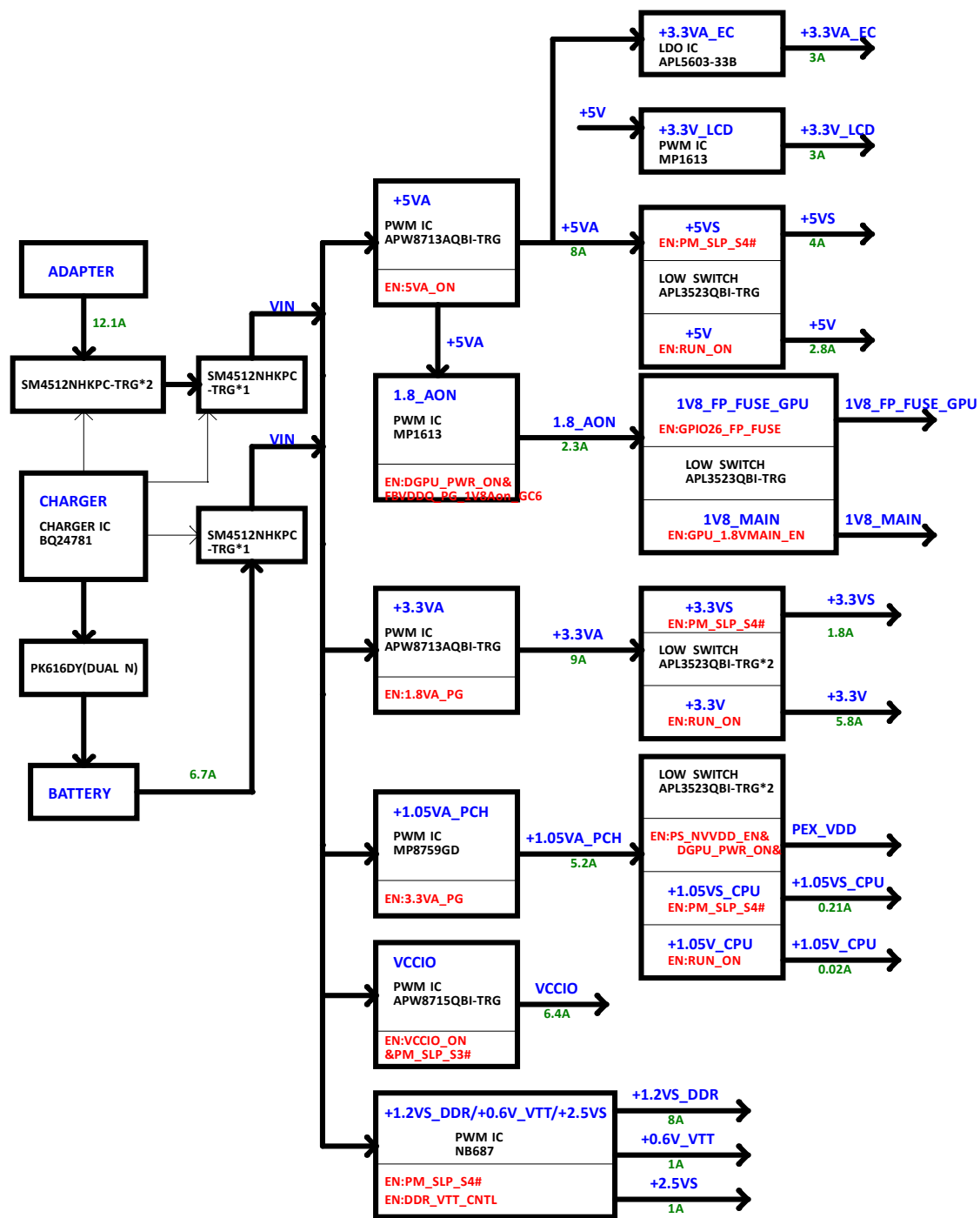
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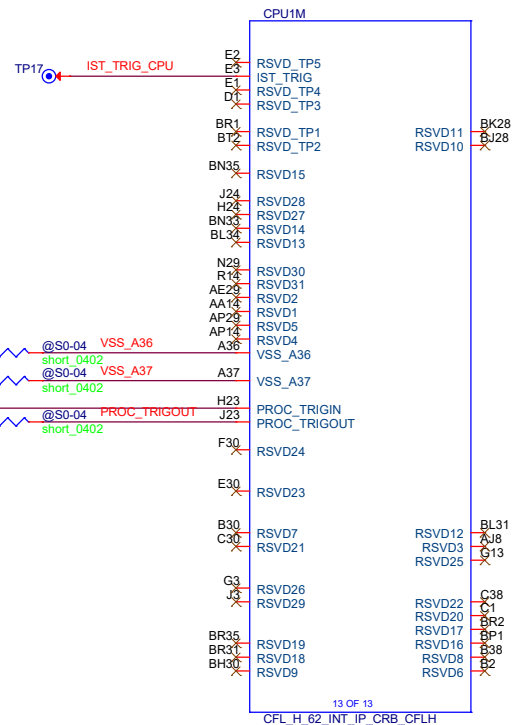
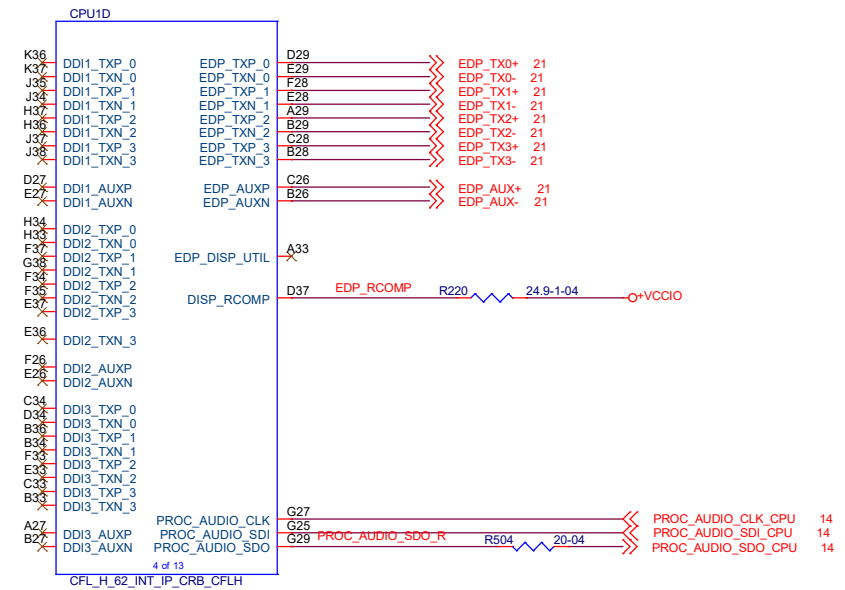
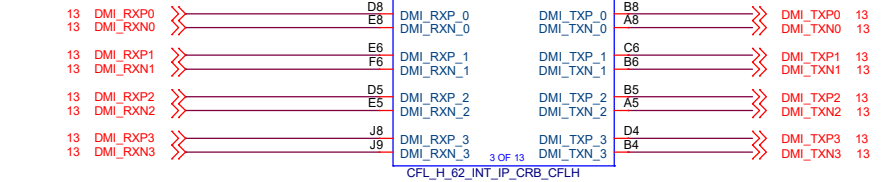
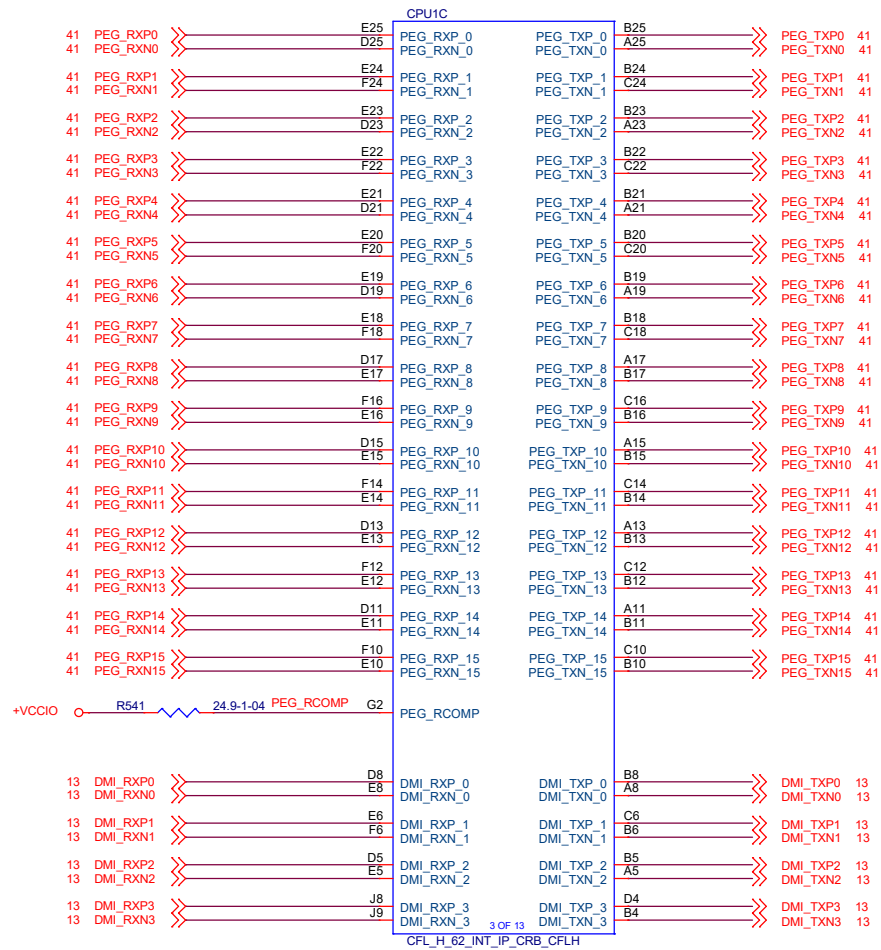
SYSTEM BLOCK DIAGRAM

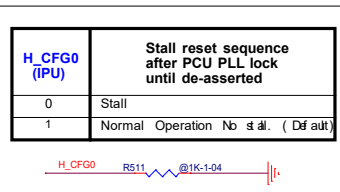
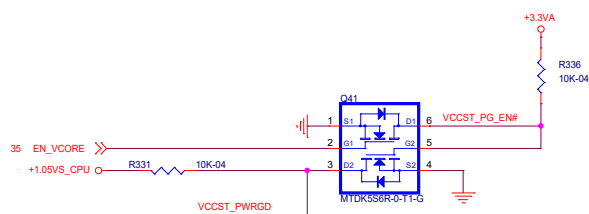
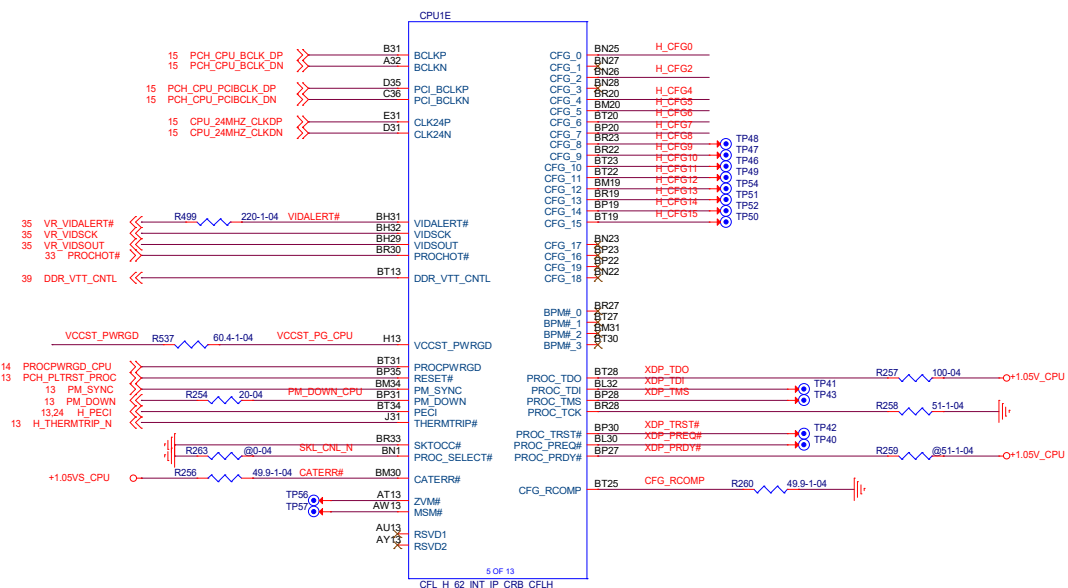


POWER ON SEQUENCE







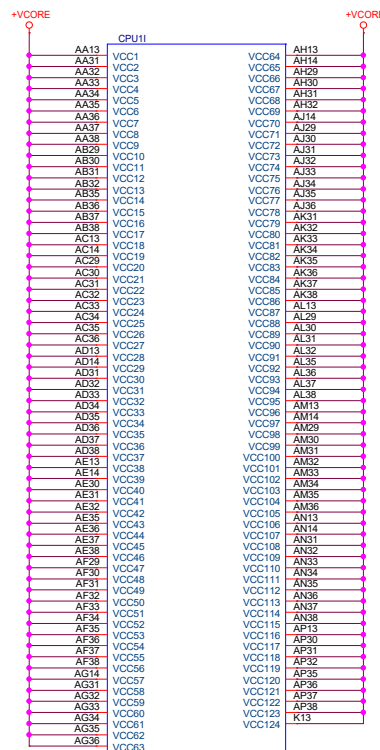
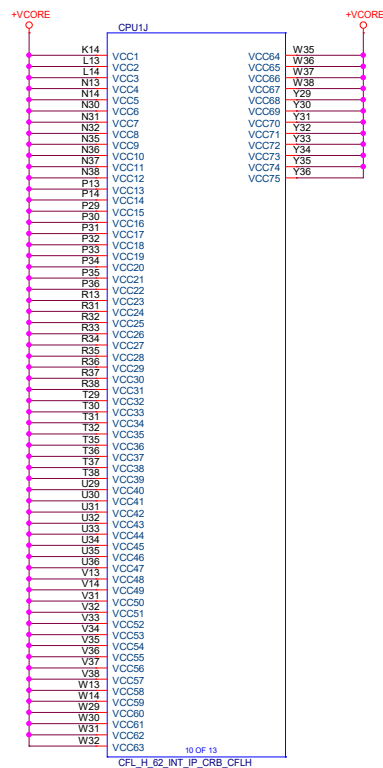


H_CFG2 (IPU)	PCI Express* Static x16 Lane Numbering Reversal
0	Lane numbers reversed
1	Normal operation

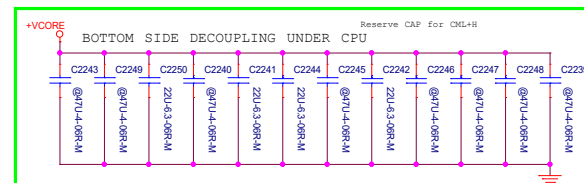
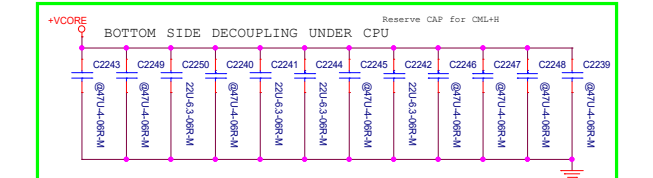
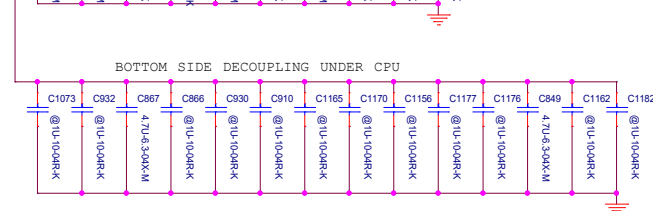
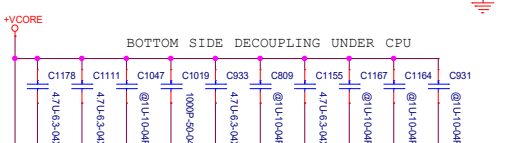
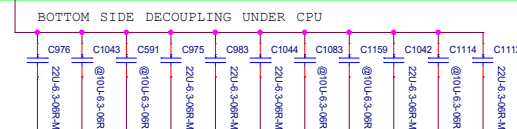
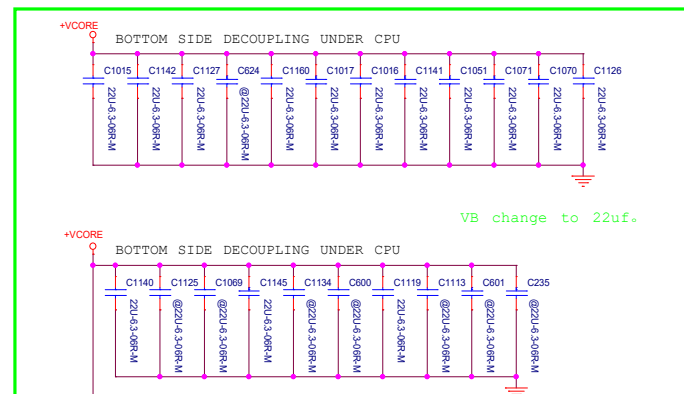
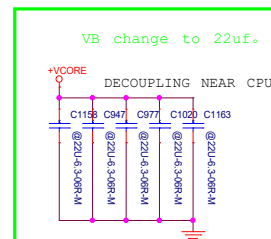
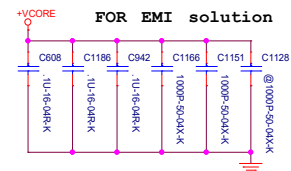
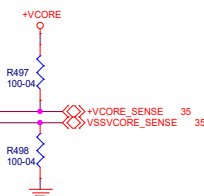
H_CFG4 (IPU)	eDP Presence strap
0	Enabled
1	Disabled

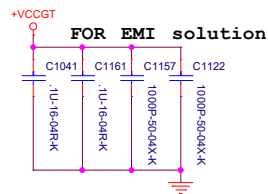
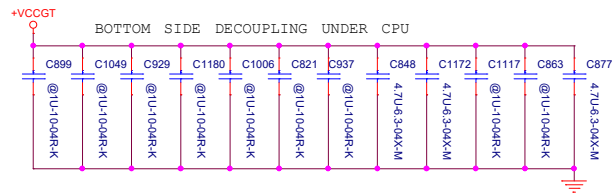
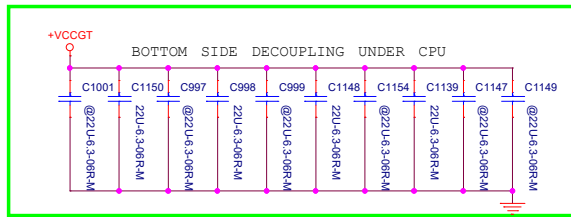
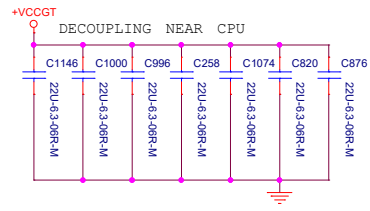
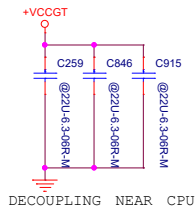
H_CFG6 (IPU)	H_CFG5 (IPU)	PCI Express* Bifurcation
0	0	1 x8, 2 x4 PCI Express
0	1	reserved
1	0	2 x8 PCI Express
1	1	1 x16 PCI Express

H_CFG7 (IPU)	PEG Training
0	PEG Wait for BIOS for training
1	PEG Train immediately following RESET# de assertion (Default)



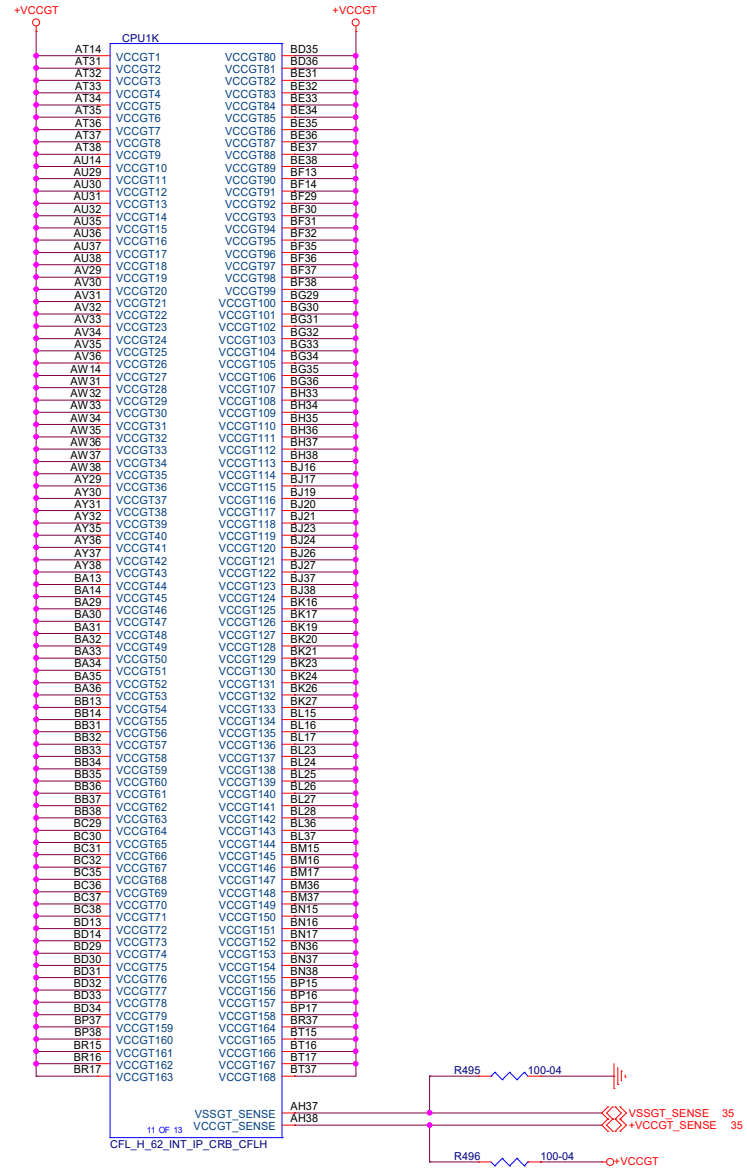
571391_CFL_PDG_V0.71
VCC
Under CPU
12 x 0603 22uF
21 x 0402 10uF
24 x 0201 1uF
24 x 0201 N/A
Near CPU
5 x 0805 47uF





611586_CML_H_PDG_Rev0p9
VCCGT
Bulk Decoupling Example
2 x 220uF
Processor Decoupling Requirements
3x 47uF 0805
7x 22uF 0402
10x 10uF 0402
12x 1uF 0201/0402

VccGT
Page 9 : 22u * 20 + 4.7u * 12 = 496.4uF
Page 36 : 22u*6 +330u*2 =792uF
Total : 1288.4uF (spec : 847uF)



611586_CML_H_PDG_RevOp9
VccIO
Bulk Decoupling Example

Processor Decoupling Requirements

VccIO
Page 10 : $22\mu \times 2 + 10 \times 1 = 54\mu\text{F}$
Page 40 : $22\mu \times 4 = 88\mu\text{F}$
Total : 142uF (CML-H spec : 124uF)

611586_CML_H_PDG_RevOp9
VccSA
Bulk Decoupling Example
Processor Decoupling Requirements

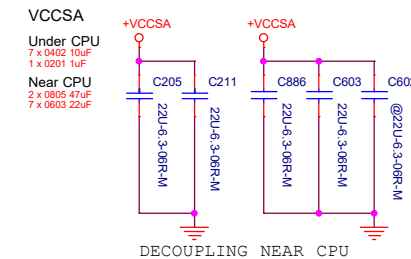
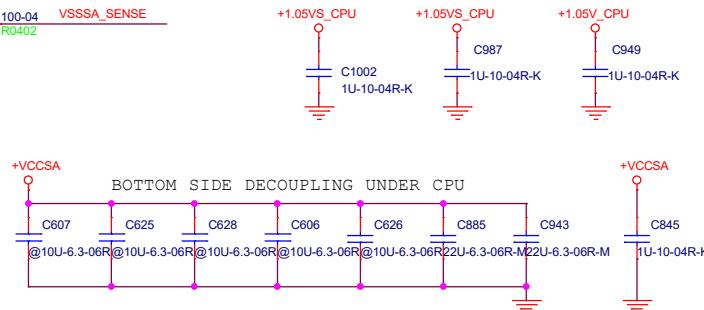
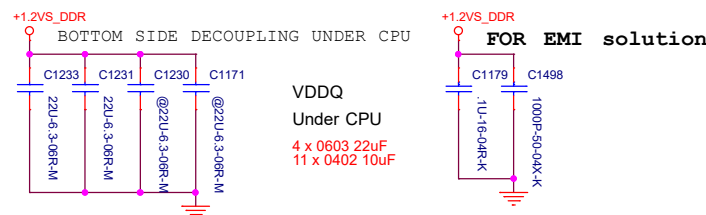
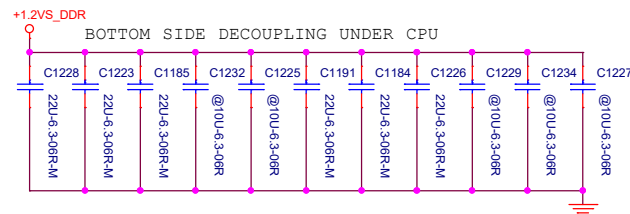
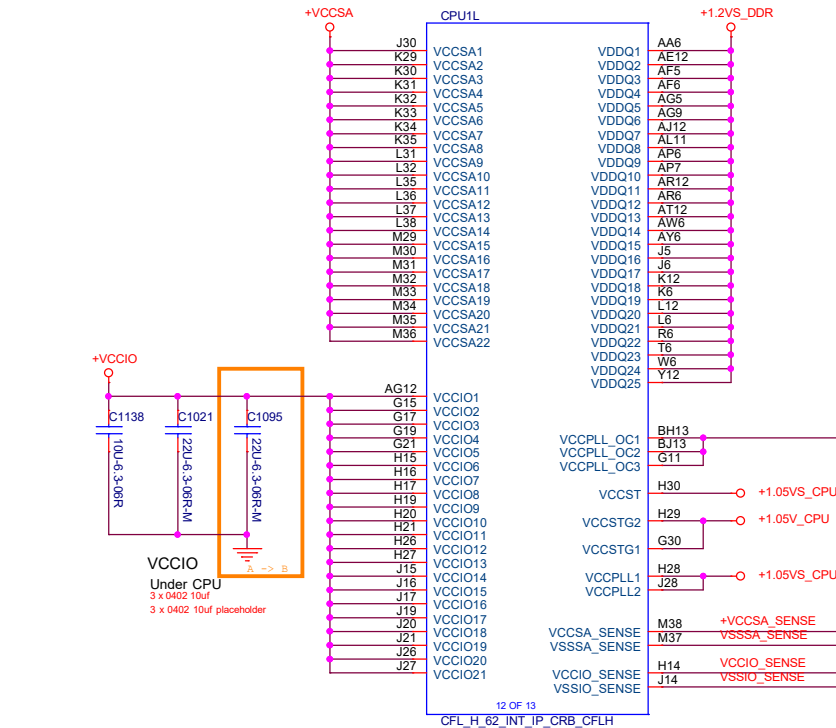
 $2 \times 47\mu\text{F } 0805$
 $1 \times 220\mu\text{F}$
Processor Decoupling Requirements

 $2 \times 47\mu\text{F } 0805$
 $2 \times 22\mu\text{F } 0603$
 $7 \times 10\mu\text{F } 0402$
 $1 \times 1\mu\text{F } 0201/0402$

VccSA
Page 10 : $47\mu \times 12 = 564\mu\text{F}$
Page 36 : $22\mu \times 4 = 88\mu\text{F}$
Total : 654uF (spec : 523uF)

611586_CML_H_PDG_RevOp9
Processor Decoupling Requirements
VDDQ
 $4 \times 22\mu\text{F } 0603$
 $1 \times 1\mu\text{F } 0201/0402$
VccSTG
 $1 \times 1\mu\text{F } 0201/0402$
VccPLL
 $1 \times 1\mu\text{F } 0201/0402$
 $1 \times 22\mu\text{F } 47\mu\text{F } 0805$
VccPLL_OC
 $2 \times 1\mu\text{F } 0201/0402$

VDDQ
Page 10 : $22\mu \times 15 = 330\mu\text{F}$
Total : 330uF (spec : 198uF)



VCCST
Under CPU
 $1 \times 0201 \ 1\mu\text{F}$

VCCSTG
Under CPU
 $1 \times 0201 \ 1\mu\text{F}$

VCCPLL
Under CPU
 $1 \times 0201 \ 1\mu\text{F}$

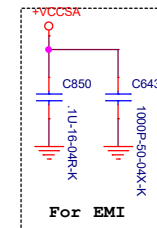
VCCPLL_OC
Under CPU
 $2 \times 0201 \ 1\mu\text{F}$

VCCPLL_OC:
CPU digital PLL power rails
VCCPLL:
CPU PLL power rails

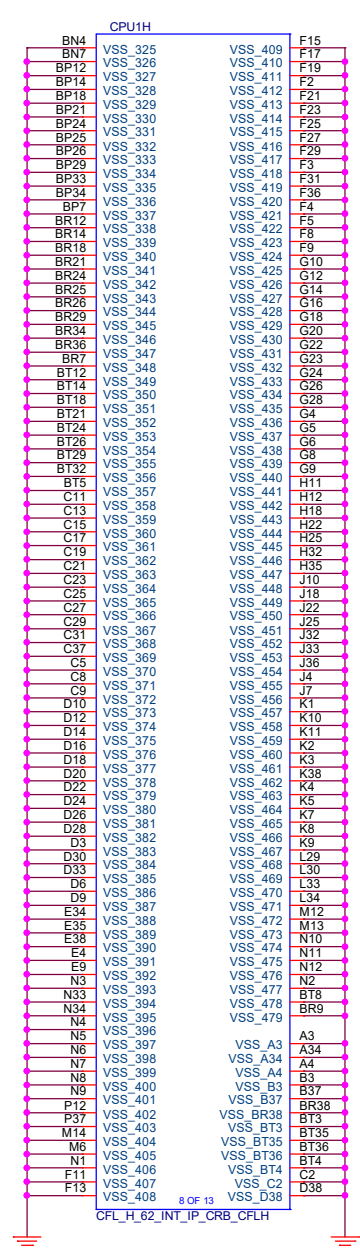
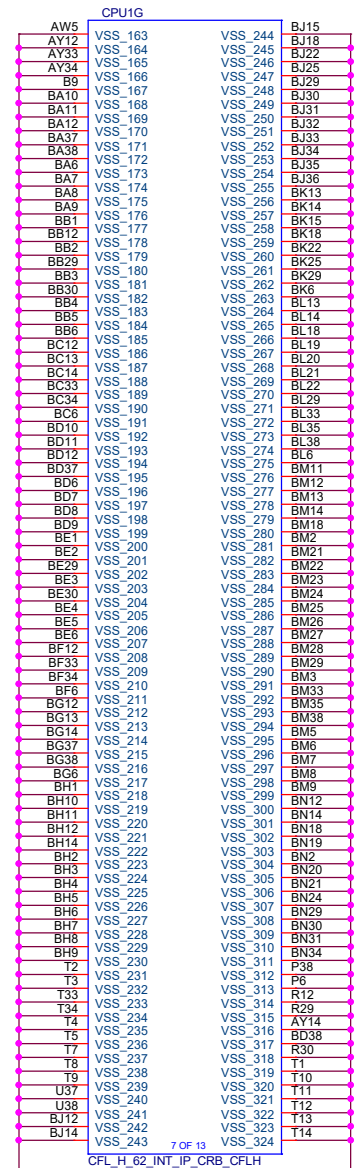
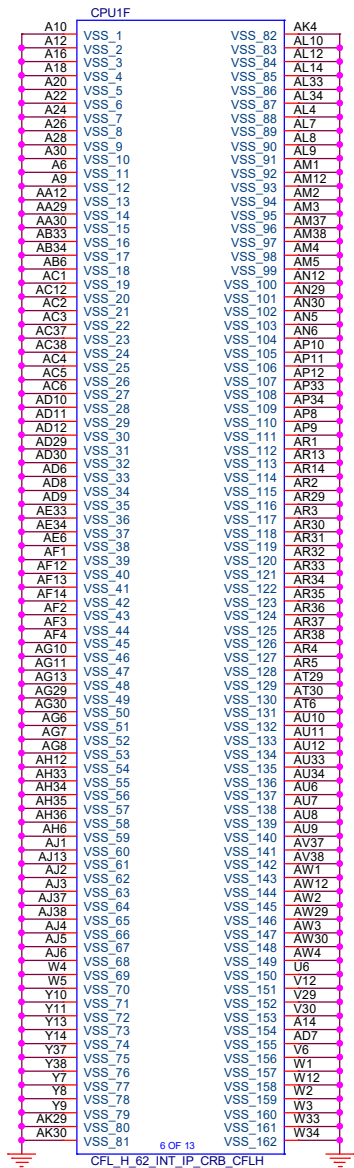
VCCST:
Sustain voltage for processor
in Standby modes
VCCSTG:
Gated version of VCCST

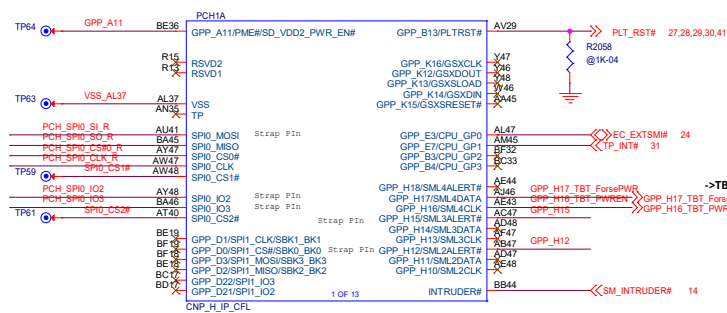
(1)VCCPLL is allowed to be OFF in S3,
but it is generally assumed to be ON
since it is powered from the same
source as VCCST.

(2) VCCPLL_OC is allowed to be turned
off during S3 if it is not powered
directly from VDDQ



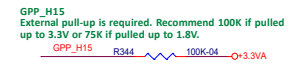
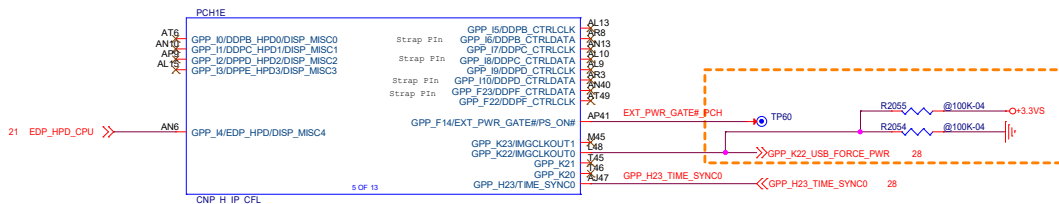
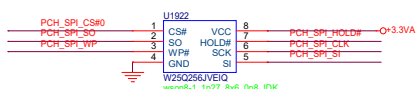
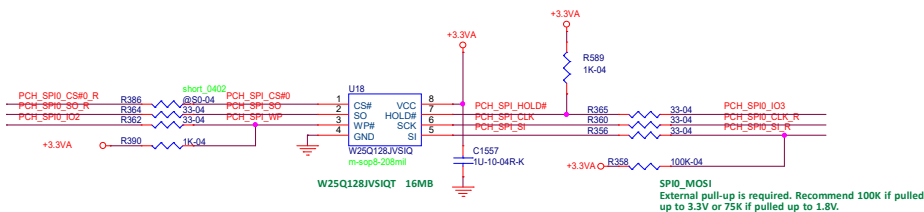
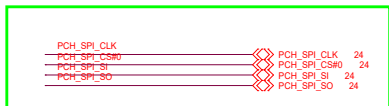
同方国际信息技术有限公司





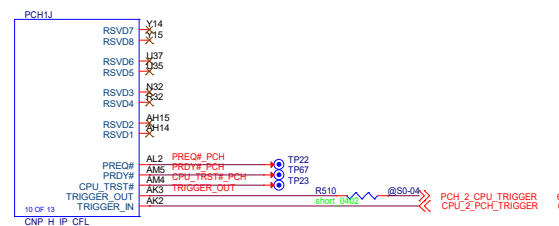
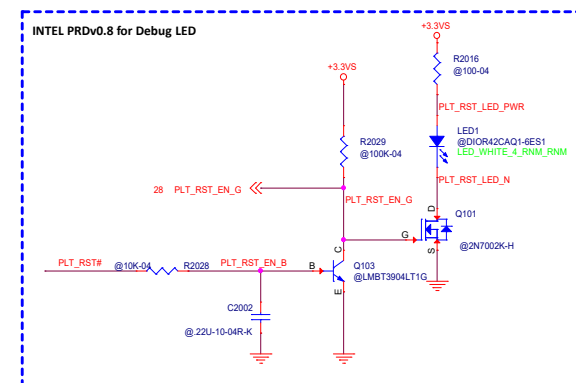
to eSPI EC

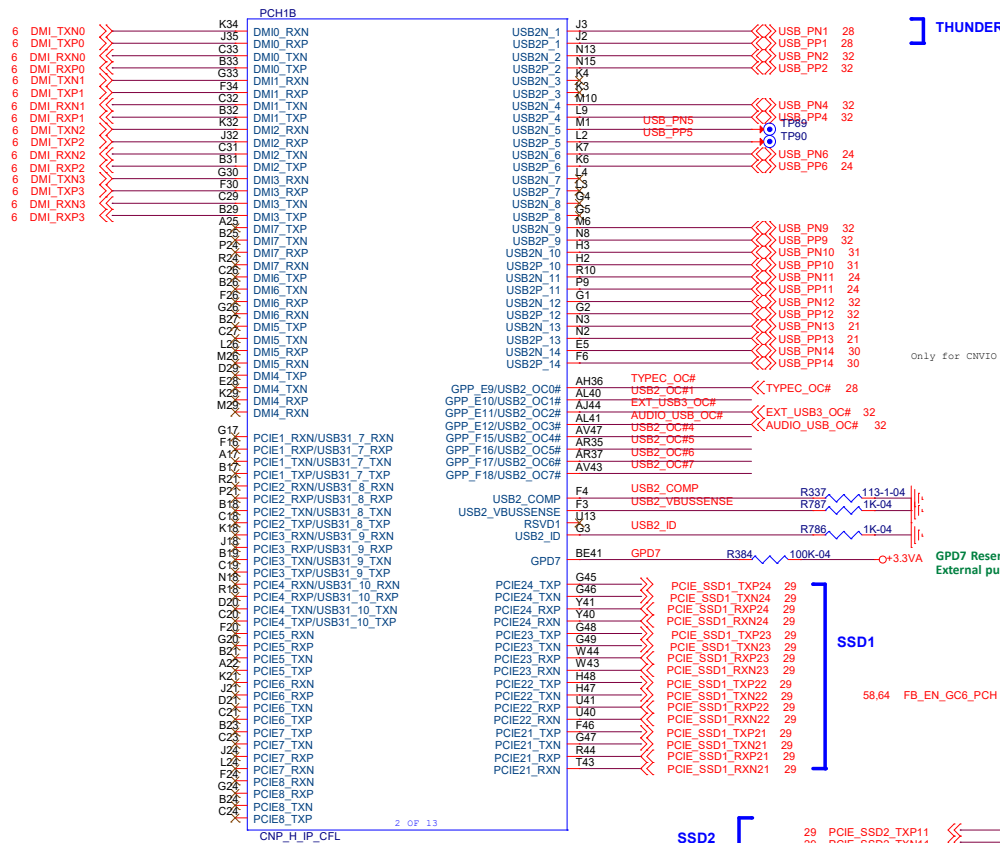
to eSPI EC



GPP_H12	eSPI Flash Sharing Mode
0	Master Attached Flash Sharing (MAFS) enabled (Default)
1	Slave Attached Flash Sharing (SAFS) enabled

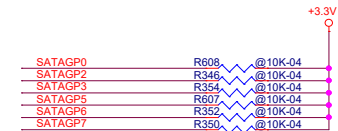
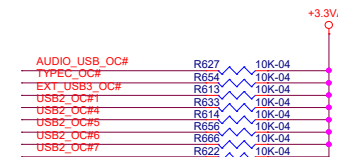
GPP_H12 R342 @4.7K-04 0+3.3V





THUNDERBOLT

USB2.0 Configuration Table	
USB1	THUNDERBOLT
USB2	CardReader on USB3.0 DB
USB3	N/A
USB4	USB3.0 Port1 on USB3.0 DB
USB5	
USB6	ME Keyboard CONN
USB7	N/A
USB8	N/A
USB9	USB3.0 Port2 on USB3.0 DB
USB10	CNFP1: Finger Print
USB11	ME Keyboard CONN
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth



Only for CNVIO

GPDP7 Reserved External pull-up is required. Recommend 100K.

SSD1

58.64 FB_EN_G6_PCH

SSD2

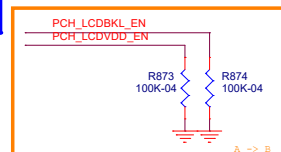
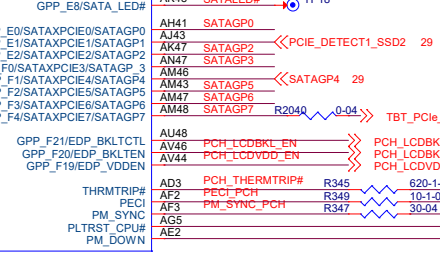
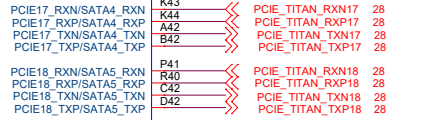
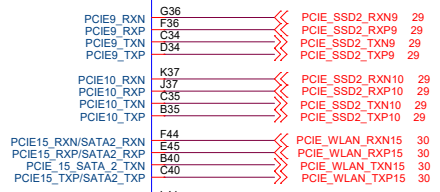
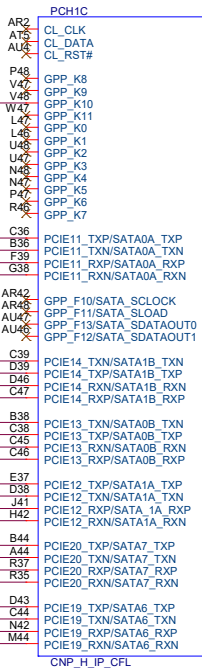
LAN

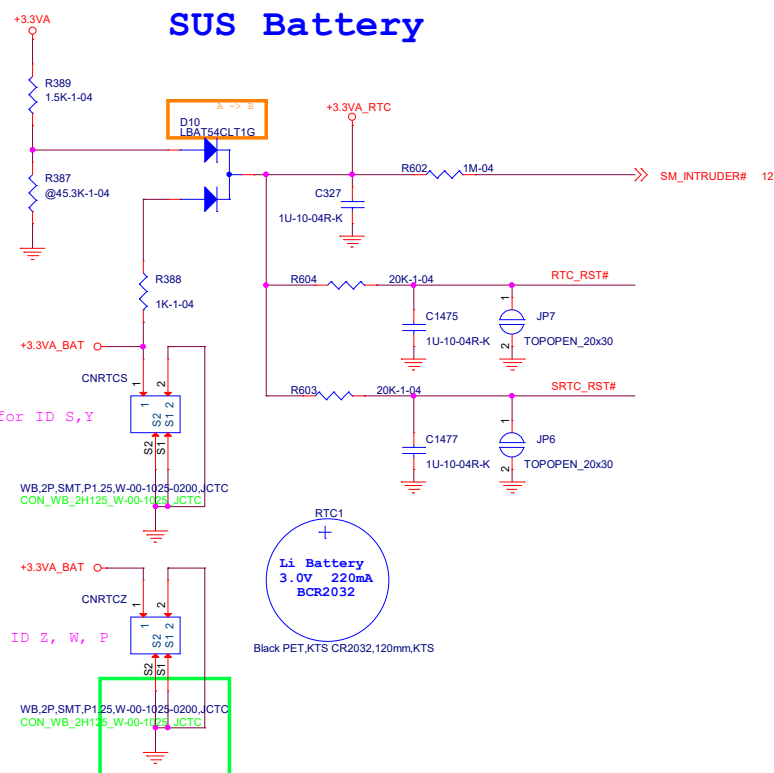
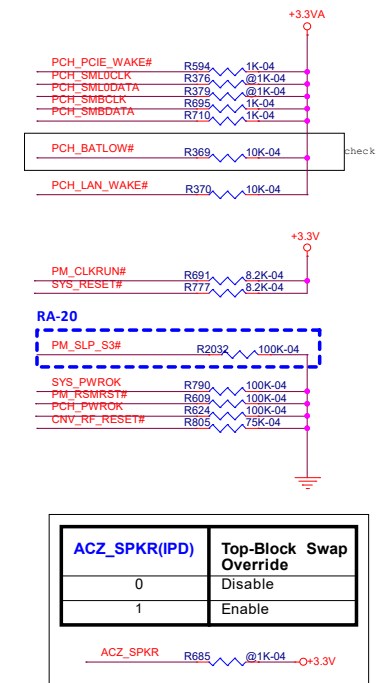
HDD

SSD2

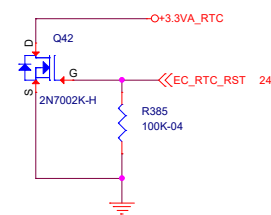
Thunderbolt

PCIe Configuration Table			
PCIe9			
PCIe10	SSD2		RST PCIe*4
PCIe11			
PCIe12			
PCIe13	HDD		
PCIe14	LAN		
PCIe15	WLAN		
PCIe16	N/A		
PCIe17	Thunderbolt		PCIe*4
PCIe18			
PCIe19			
PCIe20			
PCIe21			
PCIe22	SSD1		RST PCIe*4
PCIe23			
PCIe24			





ACZ_SPKR(IPD)	Top-Block Swap Override
0	Disable
1	Enable



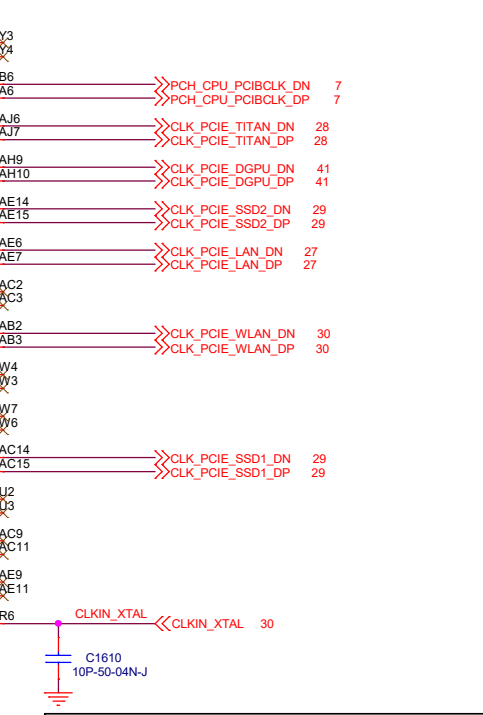
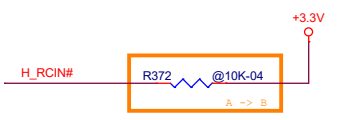
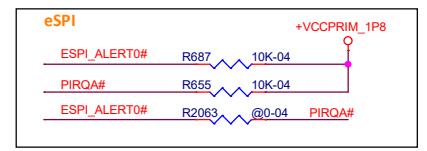
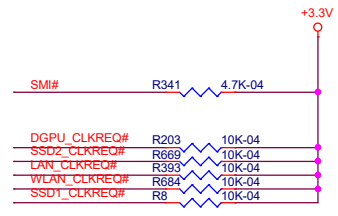
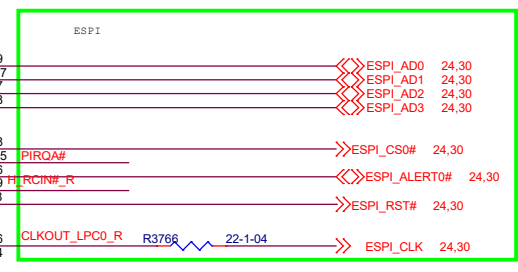
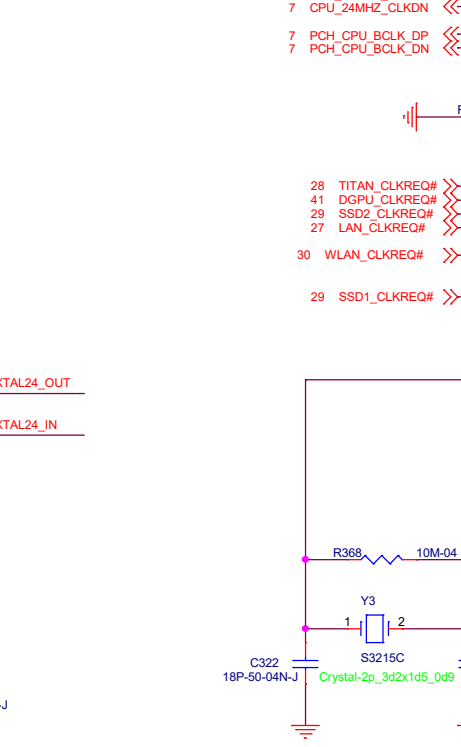
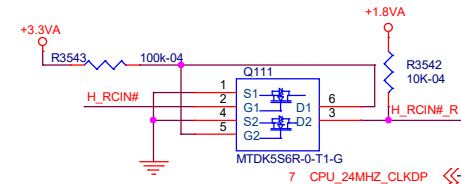
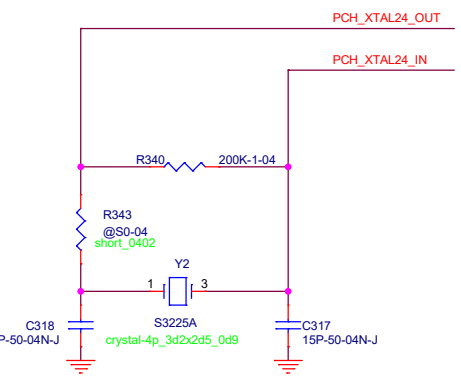
USB3.1 SD

USB3.1 USB DB

USB3.1 USB DB

USB3.1 Audio DB

USB3.0 Configuration Table	
USB3_1	N/A
USB3_2	Card Reader
USB3_3	N/A
USB3_4	USB3.1 Port Audio BD
USB3_5	USB3.0 Port1 USB DB
USB3_6	USB3.0 Port2 USB DB
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function



GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Destination
0	SPI (Default)
1	LPC

+3.3V_O R694 @150K-04 PCH_GSPI1_SI_R

GPP_B18/GSPI0_MOSI(IPD)	No Reboot Mode with TCO Disabled
0	Disabled (Default)
1	Enable

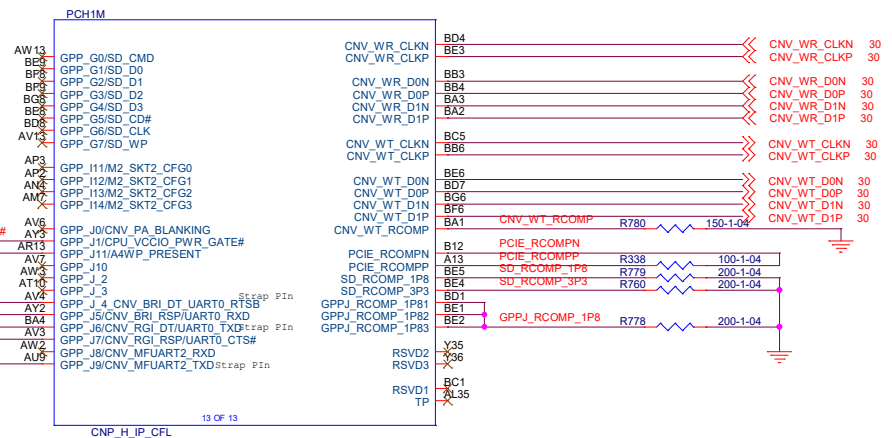
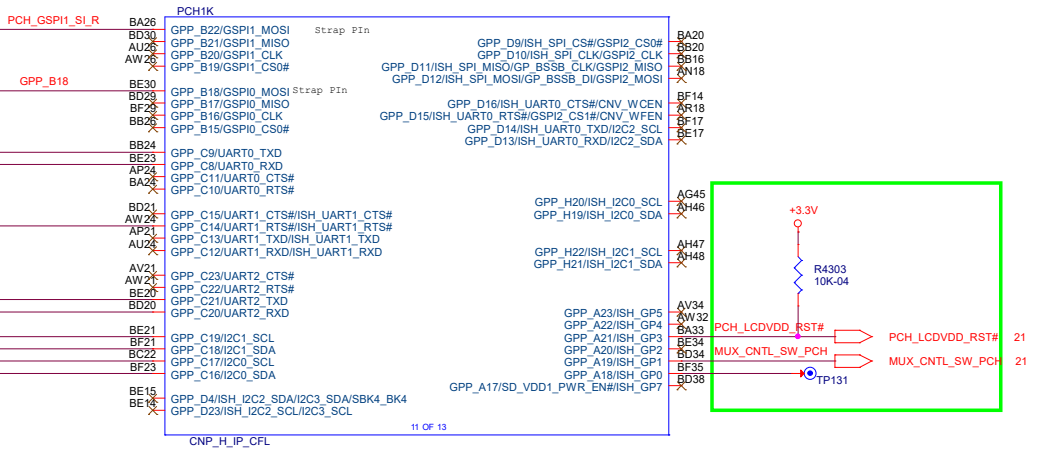
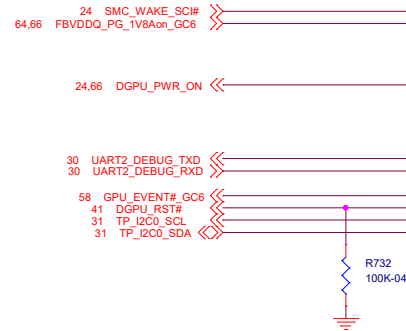
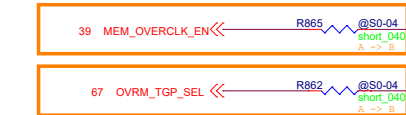
+3.3V_O R373 @4.7K-04 GPP_B18

CNV_BRI_DT (IPD)	XTAL Frequency Select
0	38.4MHz XTAL frequency
1	24MHz XTAL frequency (Default)

+VCCPRIM_1P8 R796 10K-04 CNV_BRI_DT_PCH
B -> 1.0

CNV_RGI_DT	M.2 CNV Mode Select
0	Integrated CNVi enable
1	Integrated CNVi disable

+VCCPRIM_1P8 R795 20K-04 CNV_RGI_DT_PCH
R366 @100K-04
Close to CNVi module



GPP_J9	VCCPSPI Rail select
0	VCCPSPI is connected to 3.3V
1	VCCPSPI is connected to 1.8V

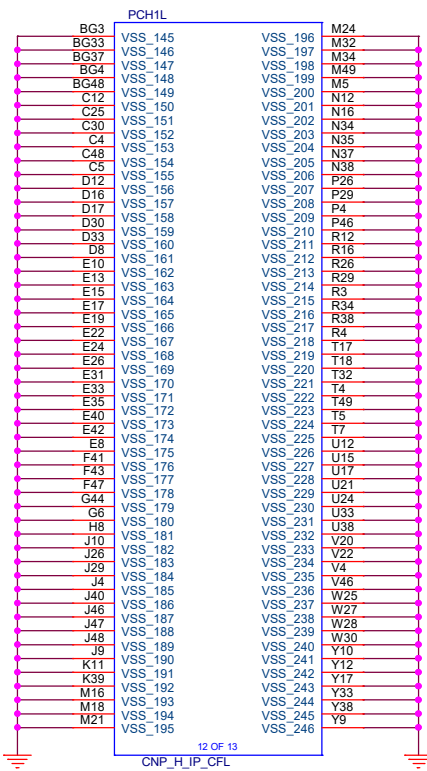
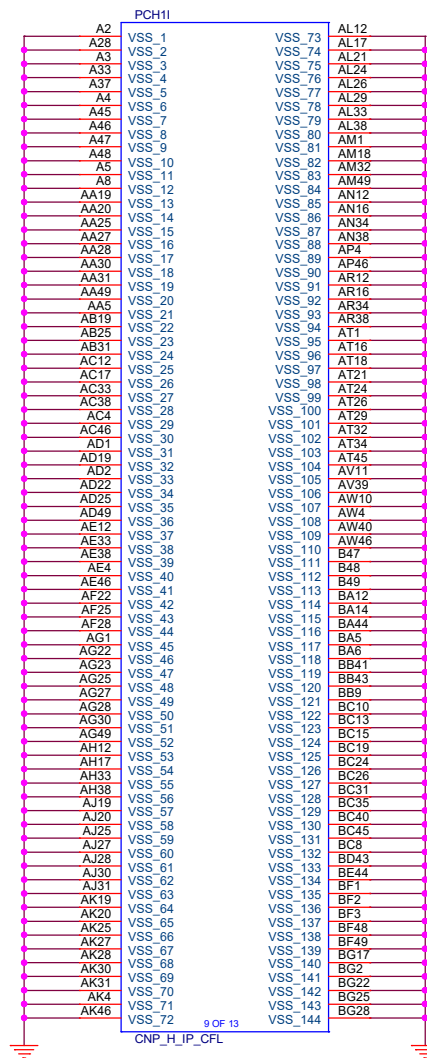
+VCCPRIM_1P8 R753 @4.7K-04 GPP_J9

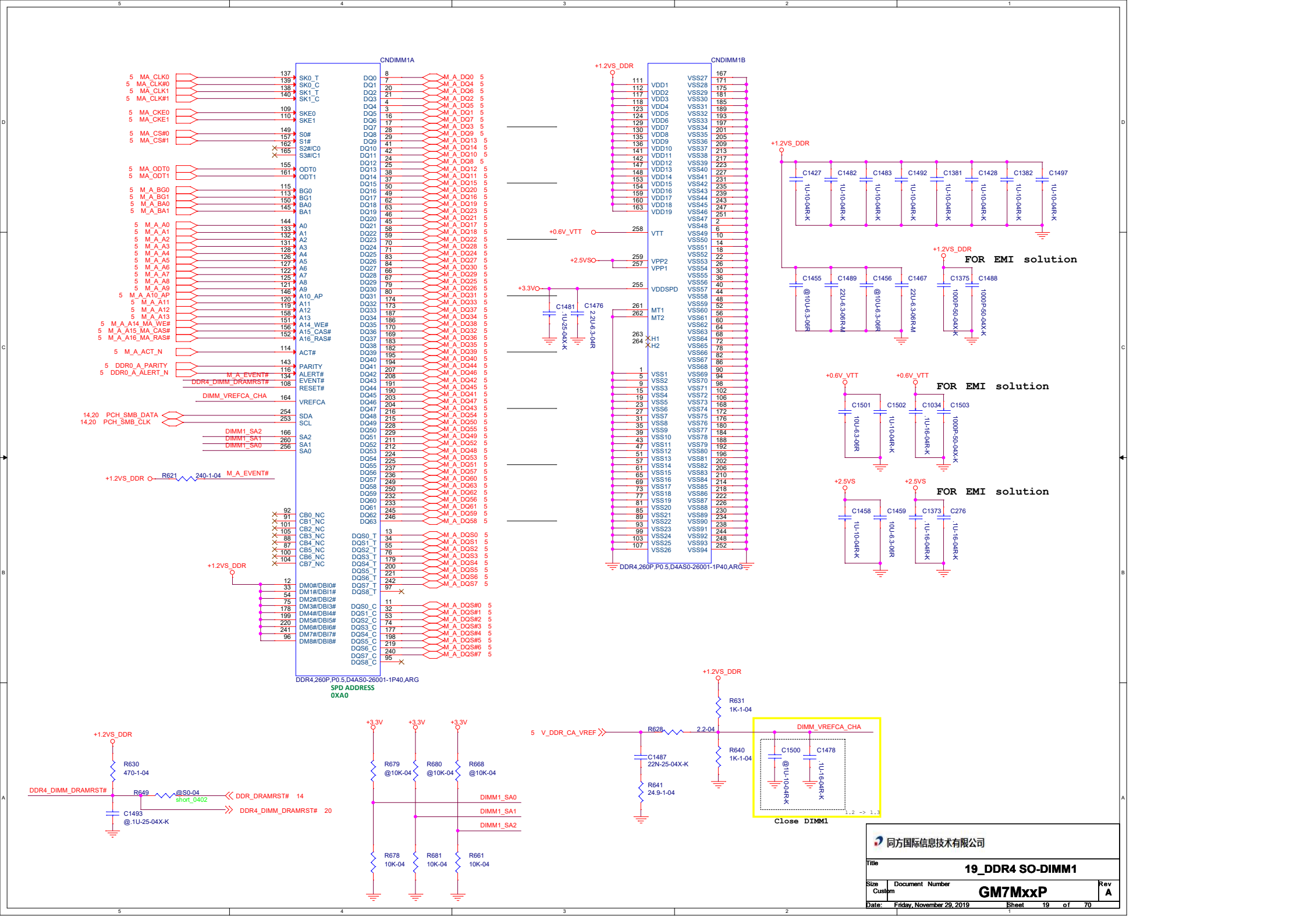
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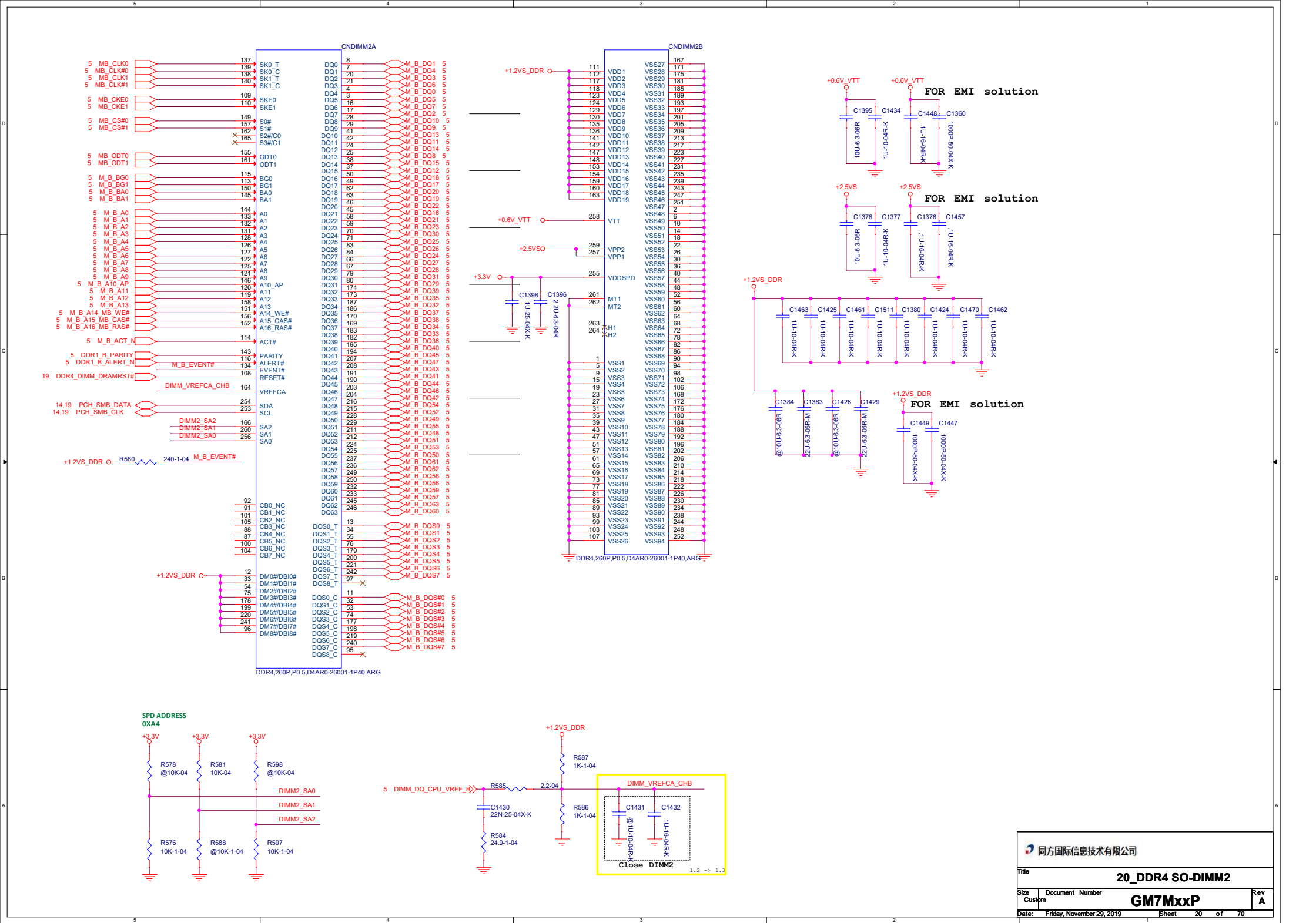
Title 16_PCH CFL-H CNVi/UART/I2C

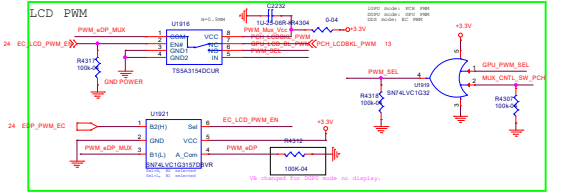
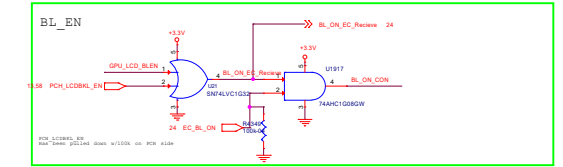
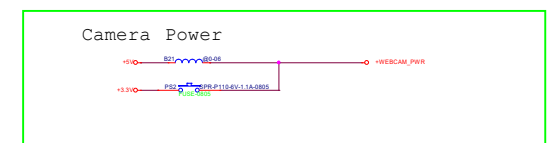
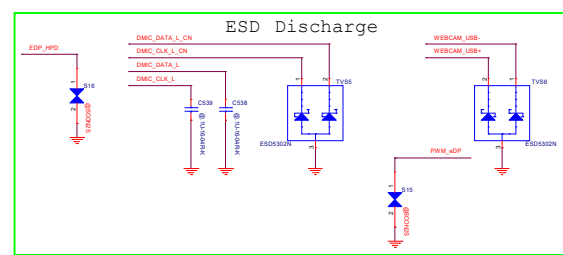
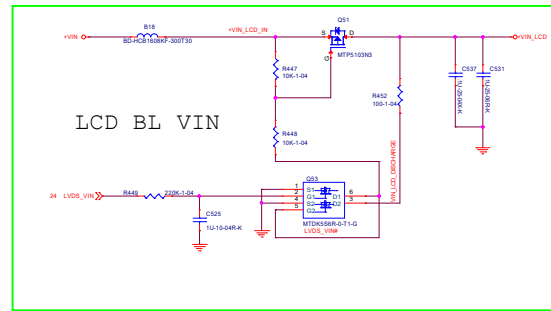
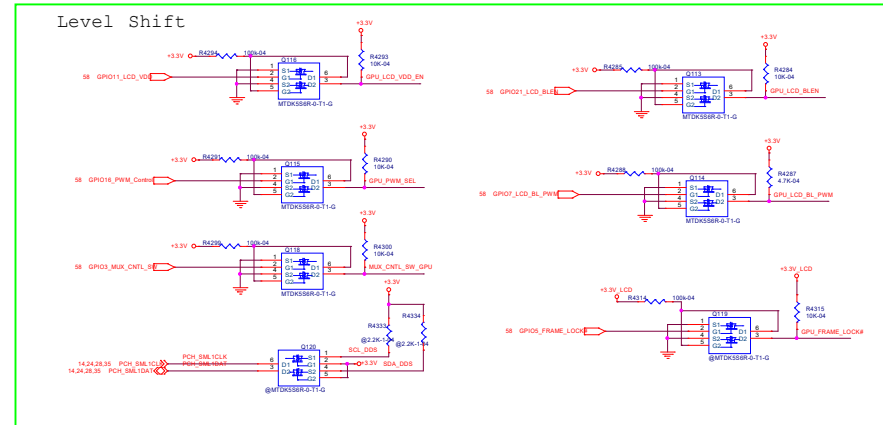
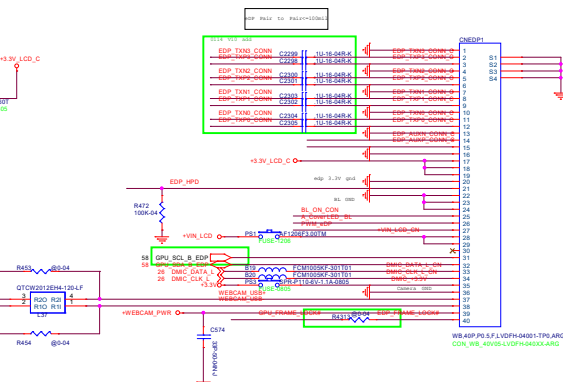
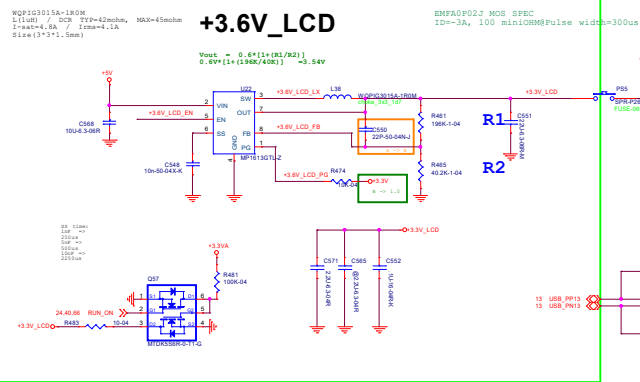
Size Document Number Custom GM7MxxP Rev A

Date: Tuesday, January 14, 2020 Sheet 16 of 70

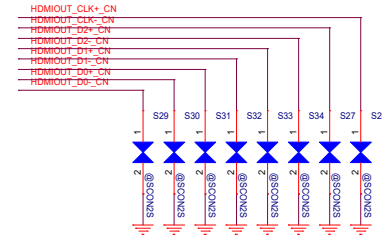




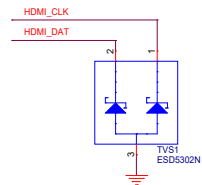




HDMI	R2.0	670MHz	NV Supported
HDMI	R1.4	340MHz	Intel Supported



CNHDMI1





D

D

C

C

B

B

A

A

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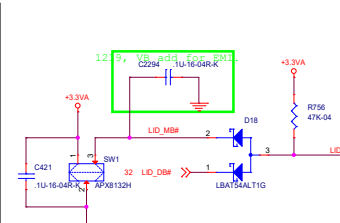
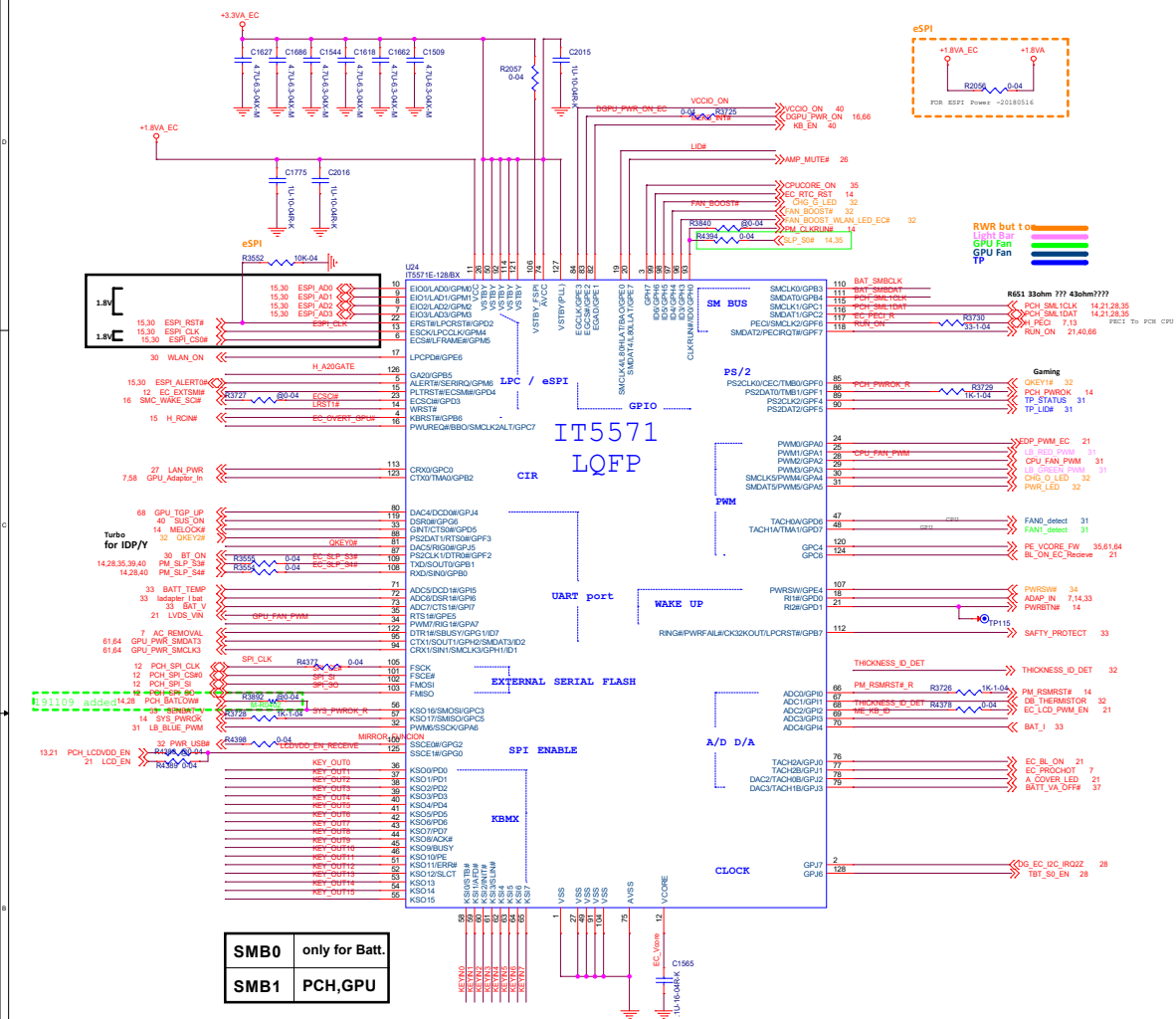
Title **23_Mini DisplayPort**

Size Custom Document Number **GM7MxxP**

Date: Thursday, November 14, 2019 Sheet 23 of 70

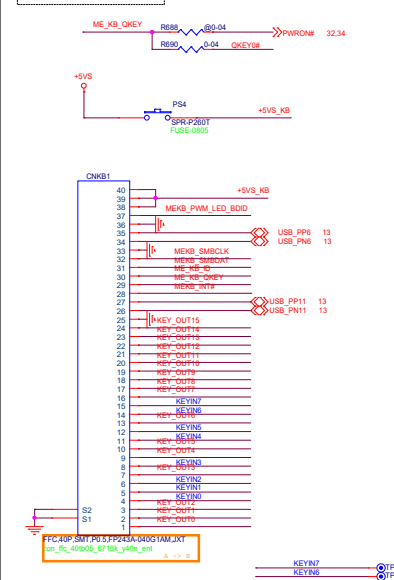
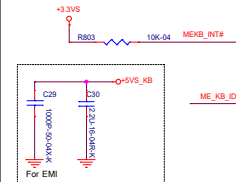
Rev **A**

EC FLASH ROM(SPI)

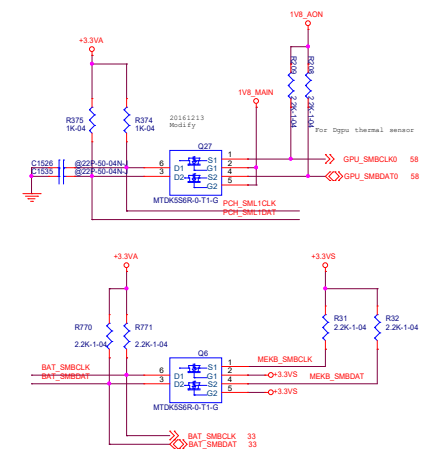


EC SMBus Distribution	
SMCLK/DAT0	Charger BAT ME KB
SMCLK/DAT1	DOS Panel 2979 Core Fov PCB GPU Temp
SMCLK/DAT2	NC
SMCLK/DAT3	GPU_SMBUS NPS2886 NPS2884

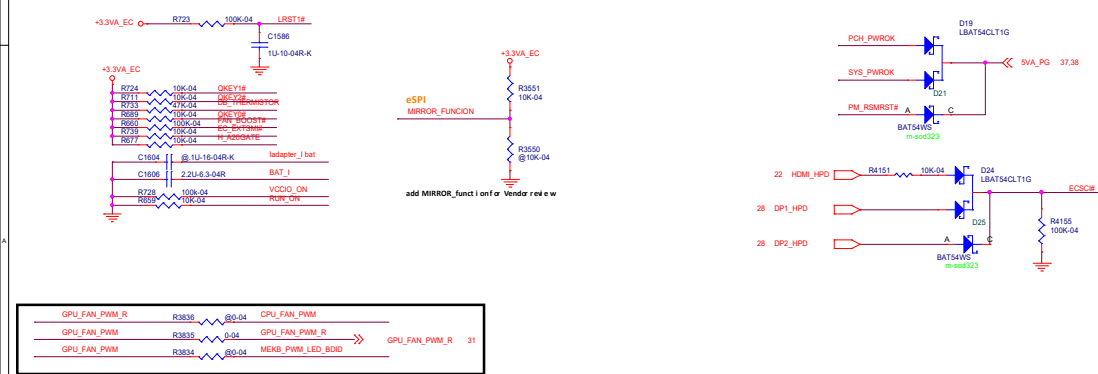
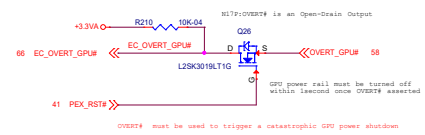
ME KEYBOARD & 4 AREA KEYBOARD



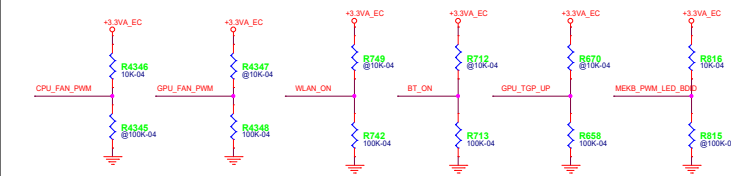
EC SMBUS LEVEL SHIFT



GPU Over Temperature Protection



Platform ID




NET Level	CFU_FAN_PWM GPA2 (12L PCB)	GPU_FAN_PWM GPA7	WLAN_ON GPE6	BT_ON GPF2	GPU_TGP GPJ4
N18E-G1-B	HIGH	LOW	LOW	LOW	LOW
N18E-G1R	HIGH	LOW	LOW	LOW	HIGH
N18E-G2R	HIGH	LOW	LOW	HIGH	LOW
N18E-G3R -MAXO	HIGH	LOW	LOW	HIGH	HIGH

D

C

B

A |

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Title

25 ME KB ESD

Size
A

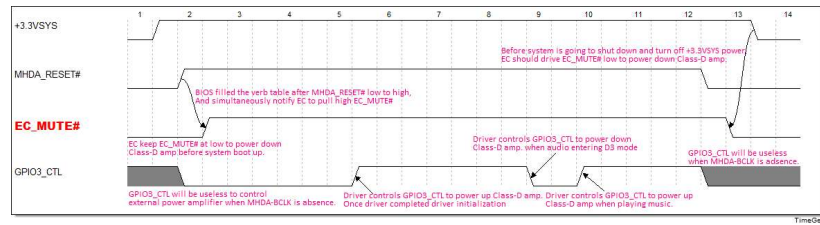
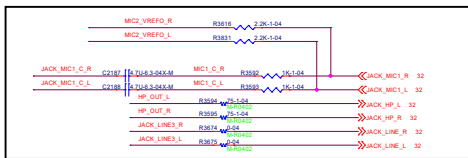
Document Number

GM7MxxP

Rev
A

Date: Thursday, November 14, 2019 Sheet 25 of 70

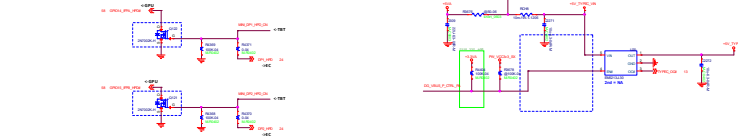
Figure 10 illustrates the power supply connections for the P10402 module. It shows three rows of connections, each corresponding to a different power unit (PU8, PU11, and PU7). Each row consists of three red lines with red circles at the input and output points. The first row for PU8 shows a +5V input connected to AB22, which is then connected to 0-04 and finally to +5V_CODEC_AVDD. The second row for PU11 shows a +1.8V input connected to AB23, which is then connected to 0-04 and finally to +1.8V_CODEC_AVDD. The third row for PU7 shows a +3.3V input connected to AB24, which is then connected to 0-04 and finally to +3.3V_CODEC_DVDD.



ALC1306-CGT

INT_SPEAKER

Pin	Function
1	AVDD
2	AVDD
3	AVDD
4	AVDD
5	AVDD
6	AVDD
7	AVDD
8	AVDD
9	AVDD
10	AVDD
11	AVDD
12	AVDD
13	AVDD
14	AVDD
15	AVDD
16	AVDD
17	AVDD
18	AVDD
19	AVDD
20	AVDD
21	AVDD
22	AVDD
23	AVDD
24	AVDD
25	AVDD
26	AVDD
27	AVDD
28	AVDD
29	AVDD
30	AVDD
31	AVDD
32	AVDD



The diagram illustrates the timing relationships for TBI ports and DP lanes. It shows multiple signal lines (TBI0-TBI15 and DP0-DP15) with various timing annotations. Key features include:

- TBI PORTS:** Signals TBI0 through TBI15 are shown. TBI0-TBI7 are labeled as "TBI0-TBI7" and TBI8-TBI15 as "TBI8-TBI15".
- DP Lanes:** Signals DP0 through DP15 are shown. DP0-DP7 are labeled as "DP0-DP7" and DP8-DP15 as "DP8-DP15".
- Timing Annotations:**
 - Setup Time:** Indicated by a blue dashed box labeled "Setup Time" for TBI0-TBI7.
 - Hold Time:** Indicated by a red dashed box labeled "Hold Time" for TBI0-TBI7.
 - Eye Diagram:** A red eye diagram is shown for TBI0-TBI7.
 - Signal Transitions:** Various signal transitions are marked with red and blue arrows.
 - Timing Constraints:** Various timing constraints are marked with red and blue arrows.
- Legend:**
 - TP SP Configuration:**
 - CS0.1 ports may be used
 - CS0.2 lanes may be used
 - DP0.2.1 ports may be used
 - DP0.2.2 lanes may be used
 - DP0.2.3 ports may be used
 - DP0.2.4 lanes may be used
 - DP0.2.5 ports may be used
 - DP0.2.6 lanes may be used
 - DP0.2.7 ports may be used
 - DP0.2.8 lanes may be used
 - DP0.2.9 ports may be used
 - DP0.2.10 lanes may be used
 - DP0.2.11 ports may be used
 - DP0.2.12 lanes may be used
 - DP0.2.13 ports may be used
 - DP0.2.14 lanes may be used
 - DP0.2.15 ports may be used
 - DP0.2.16 lanes may be used
 - CS0.1 ports may be used**
 - CS0.2 lanes may be used**
 - DP0.2.1 ports may be used**
 - DP0.2.2 lanes may be used**
 - DP0.2.3 ports may be used**
 - DP0.2.4 lanes may be used**
 - DP0.2.5 ports may be used**
 - DP0.2.6 lanes may be used**
 - DP0.2.7 ports may be used**
 - DP0.2.8 lanes may be used**
 - DP0.2.9 ports may be used**
 - DP0.2.10 lanes may be used**
 - DP0.2.11 ports may be used**
 - DP0.2.12 lanes may be used**
 - DP0.2.13 ports may be used**
 - DP0.2.14 lanes may be used**
 - DP0.2.15 ports may be used**
 - DP0.2.16 lanes may be used**

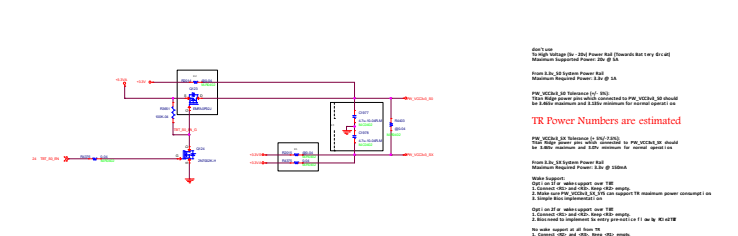
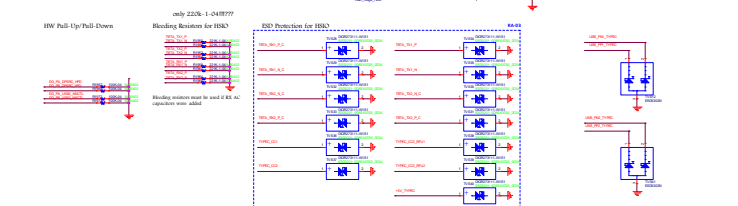


Figure 10: USB and SATA connections for the T1020

The figure consists of four sub-diagrams illustrating the connections for the T1020 module:

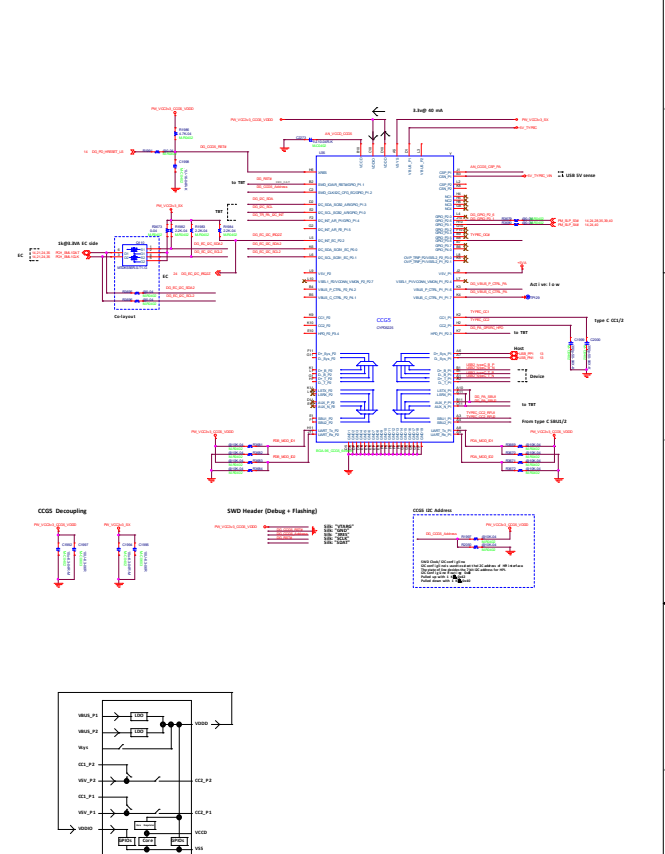
- USB Connections:** This diagram shows the connections for USB0, USB1, and USB2. It includes labels for various pins such as USB0_VBUS, USB0_DM, USB0_DP, USB1_VBUS, USB1_DM, USB1_DP, USB2_VBUS, USB2_DM, and USB2_DP. It also shows connections to the T1020 module pins.
- SATA Connections:** This diagram shows the connections for SATA0, SATA1, and SATA2. It includes labels for various pins such as SATA0_VBUS, SATA0_DM, SATA0_DP, SATA1_VBUS, SATA1_DM, SATA1_DP, SATA2_VBUS, SATA2_DM, and SATA2_DP. It also shows connections to the T1020 module pins.
- SATA Connections:** This diagram shows the connections for SATA0, SATA1, and SATA2. It includes labels for various pins such as SATA0_VBUS, SATA0_DM, SATA0_DP, SATA1_VBUS, SATA1_DM, SATA1_DP, SATA2_VBUS, SATA2_DM, and SATA2_DP. It also shows connections to the T1020 module pins.
- SATA Connections:** This diagram shows the connections for SATA0, SATA1, and SATA2. It includes labels for various pins such as SATA0_VBUS, SATA0_DM, SATA0_DP, SATA1_VBUS, SATA1_DM, SATA1_DP, SATA2_VBUS, SATA2_DM, and SATA2_DP. It also shows connections to the T1020 module pins.

Figure 1: PCB layout of the 100W GaN power converter. The figure consists of four sub-diagrams: (a) Top layer layout showing the GaN FET, gate driver, and power MOSFETs with various component footprints and labels. (b) Bottom layer layout showing the corresponding component footprints and labels. (c) Power supply decoupling circuit diagram showing the connection of the power supply to the converter, including the 100W GaN FET, gate driver, and power MOSFETs. (d) Thermal management diagram showing the placement of the 100W GaN FET, gate driver, and power MOSFETs on the PCB, with thermal vias and thermal pads indicated.

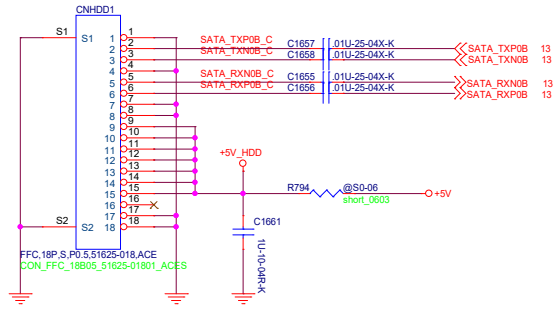
[illegible]

Interface	Description	Bit Rate
TBT	Thunderbolt™ 20Gbps channel	20.625 Gb/s
USB3.1	USB3.1 10Gbps channel	10 Gb/s
PCIe* Gen3	Used for PCIe root complex connection	8 GT/s
DisplayPort* 1.2a	Used for DP Sink connection	5.4 Gb/s
DisplayPort* 1.4 ¹	Used for DP Sink connection	8.1 Gb/s
USB* 2	Used for USB 2.0 connection	480 Mb/s

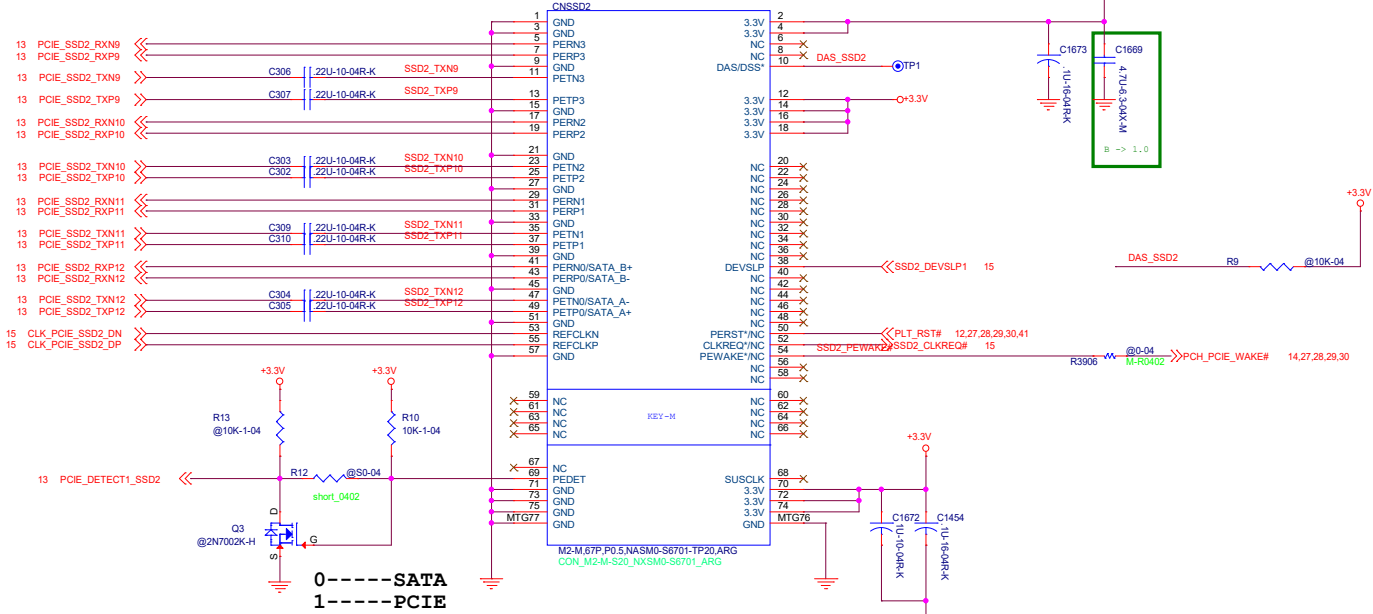
Note: 1. 8.1Gbps is only supported on Titan Ridge



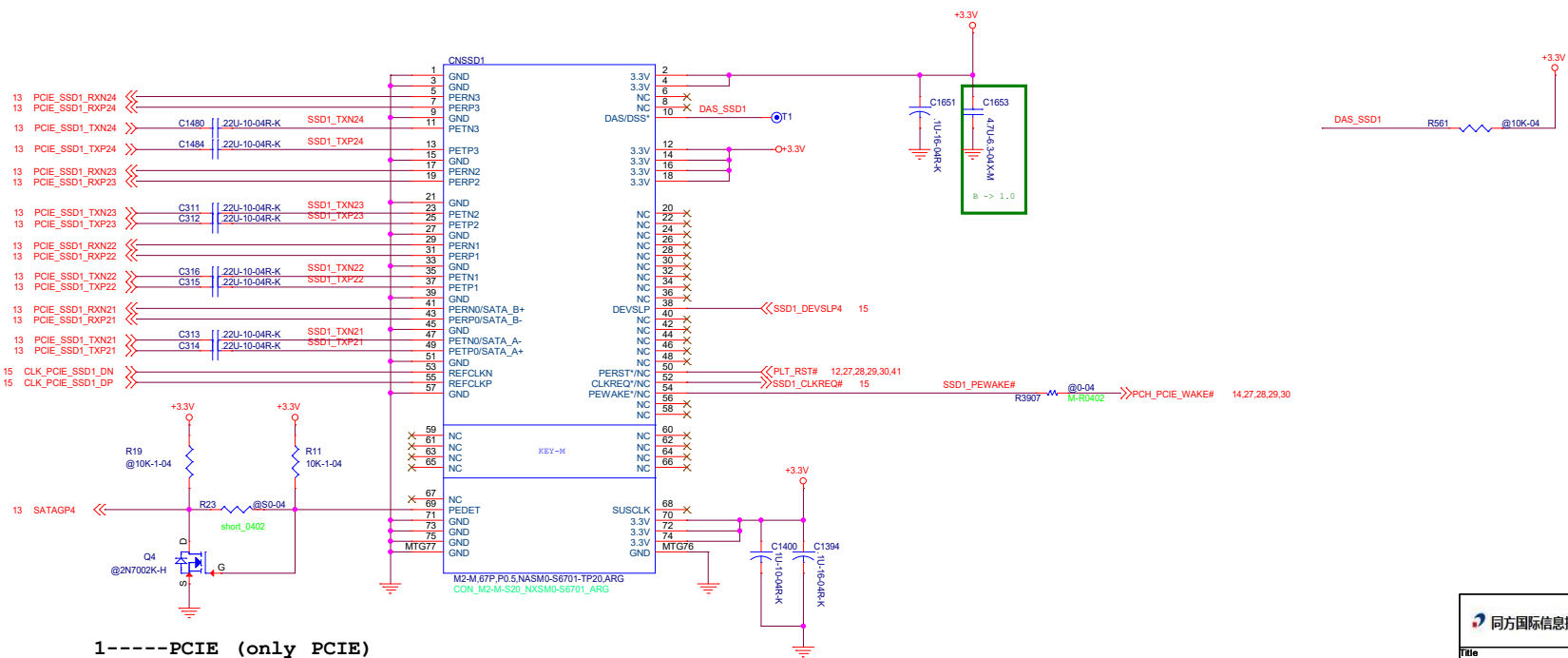
SATA-HDD



SSD2

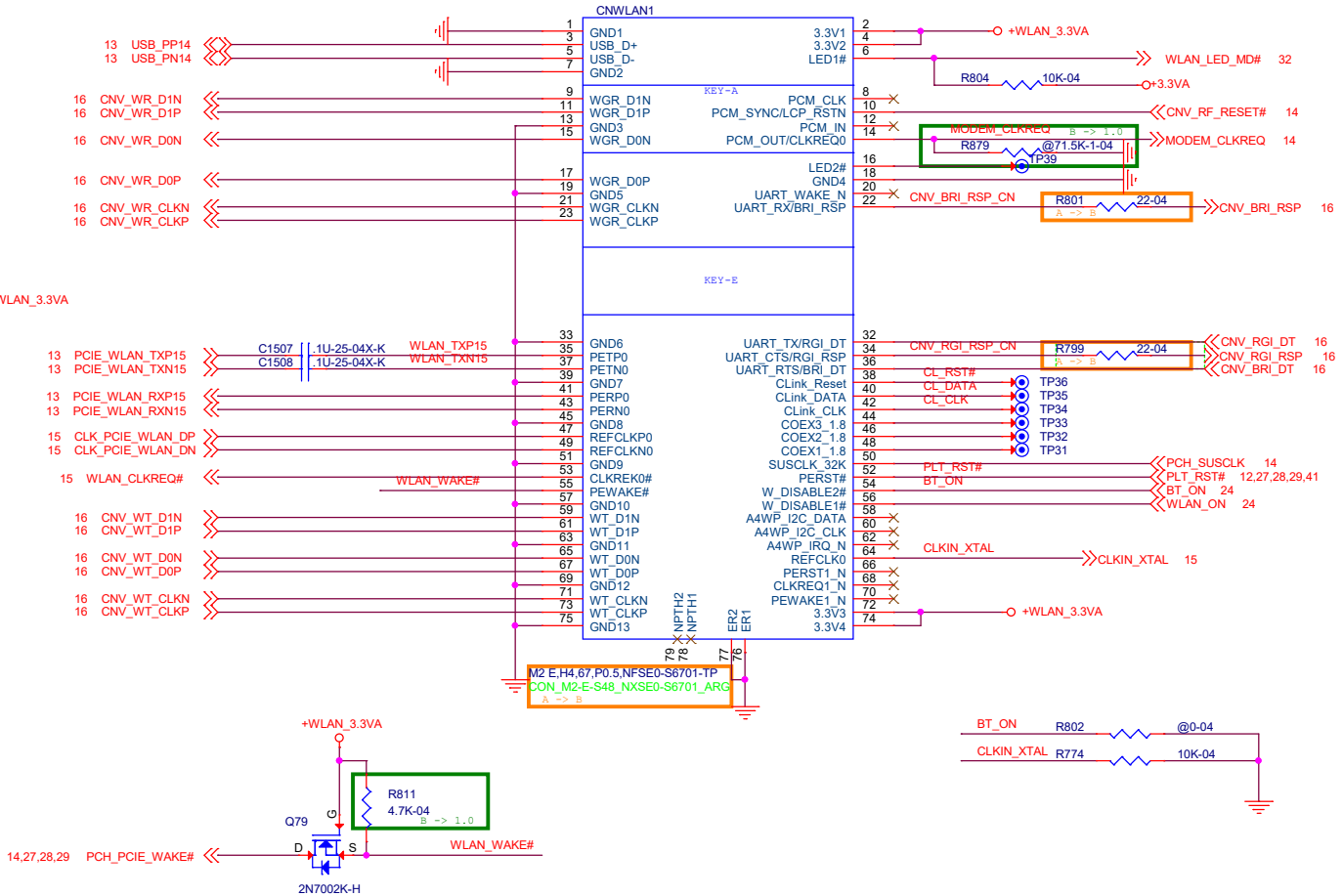
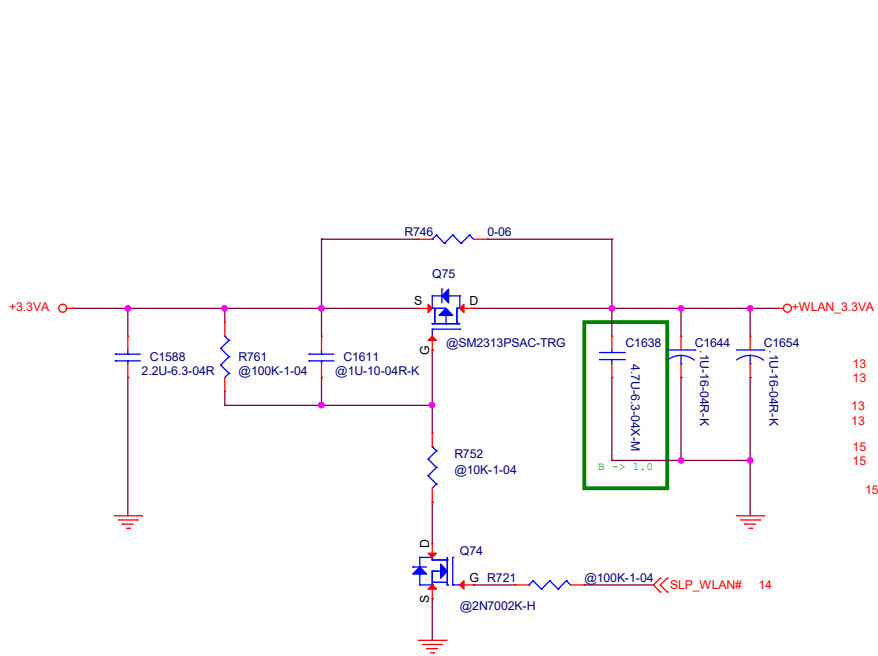


SSD1

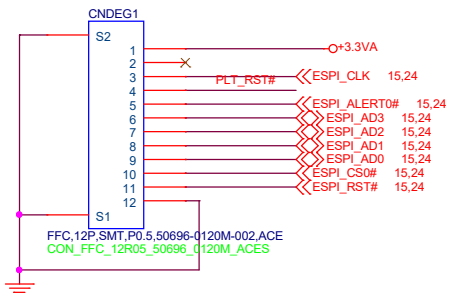


1-----PCIE (only PCIE)

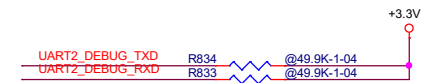
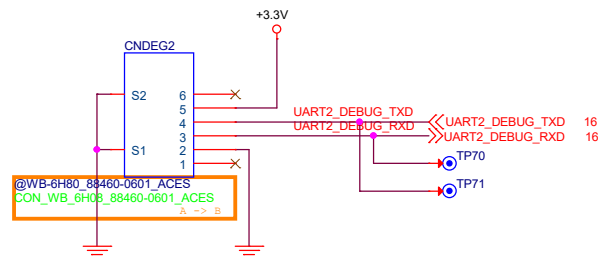
WLAN CONN



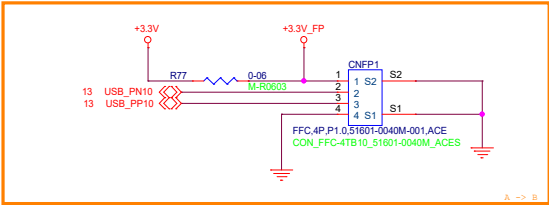
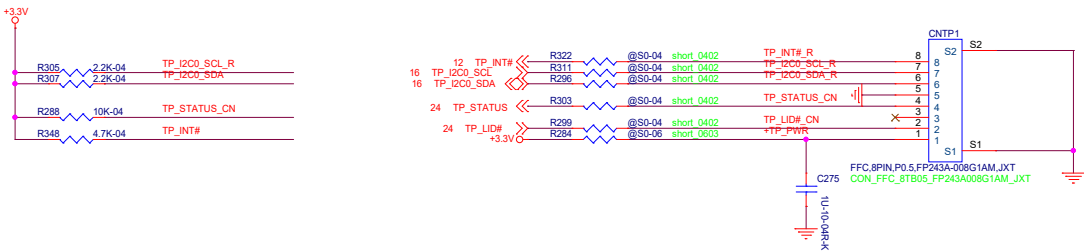
ESPI debug port



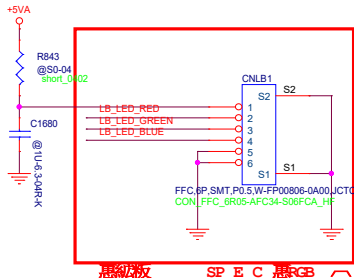
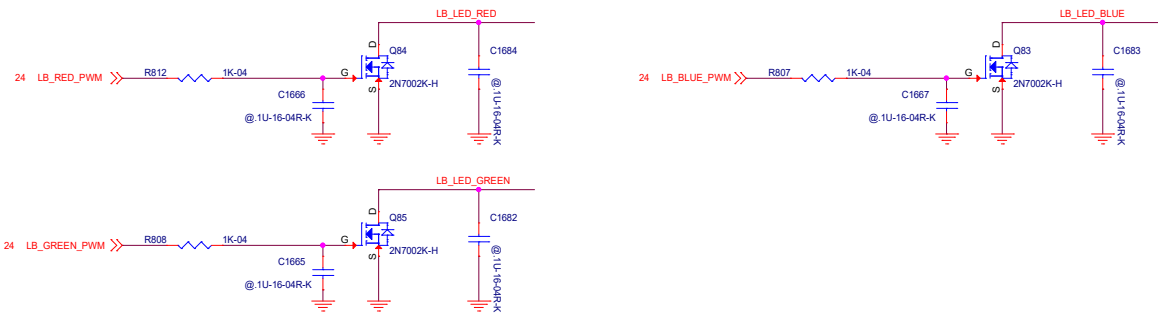
UART debug port



Touch Pad&Finger Print

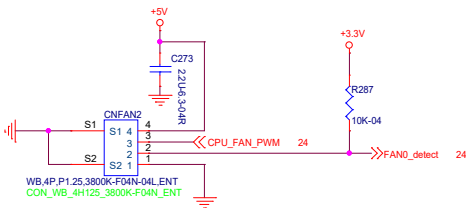


Light bar Control

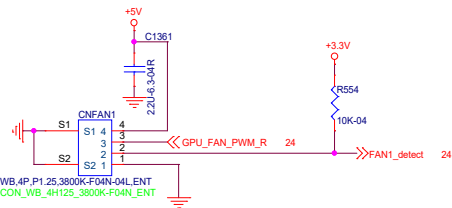


FAN CONTROLLER

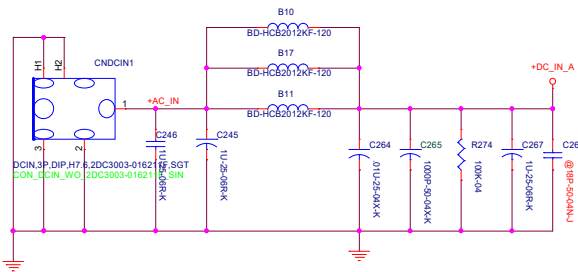
CPU FAN



GPU FAN

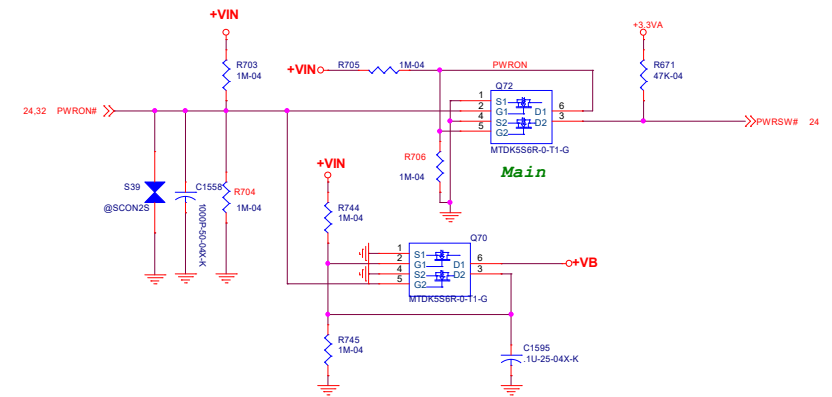


+DC_IN

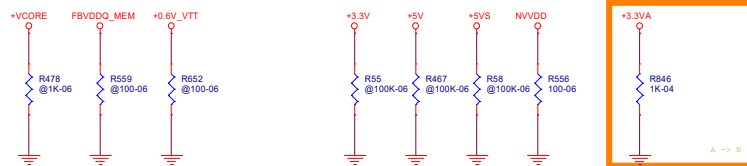


EMB20NP3V
ID=-13A TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt 0.1ms

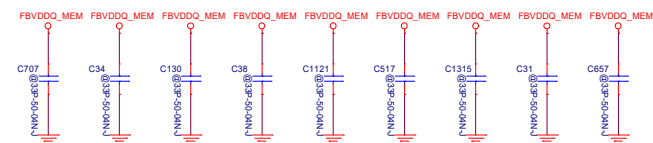
POWER SW



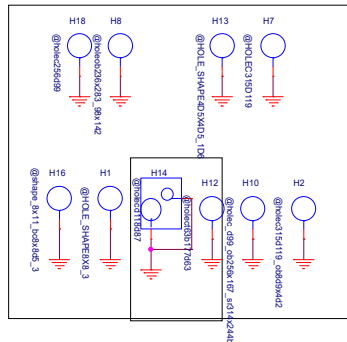
Discharge Resistor



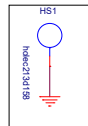
For RF



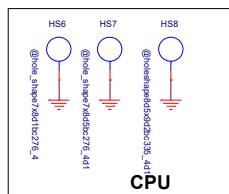
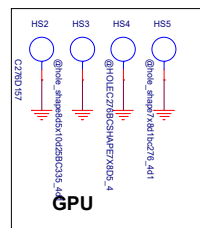
PCB HOLE



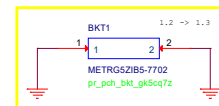
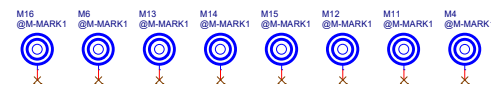
WLAN HOLE



THERMAL HOLE

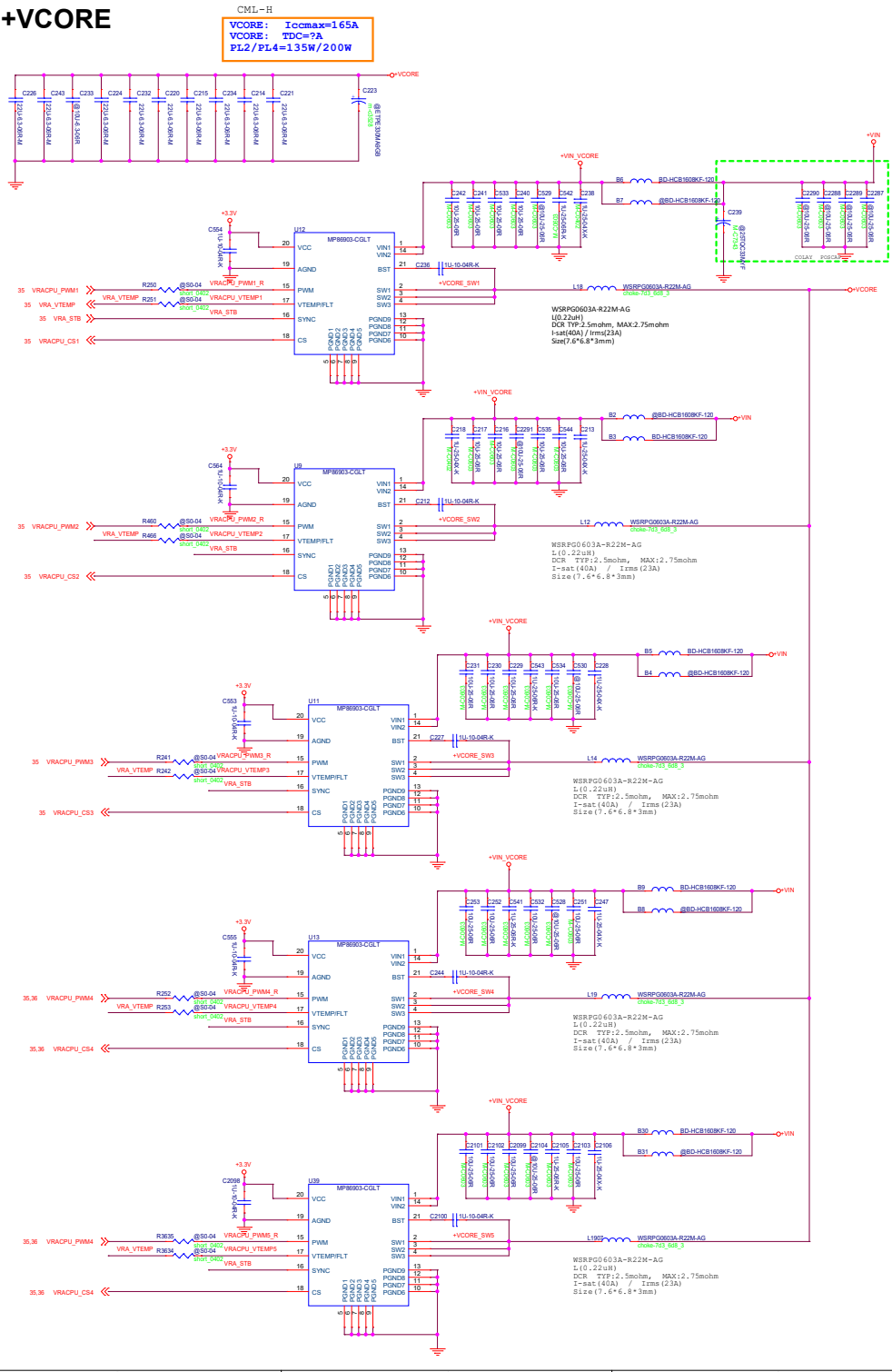


CPU

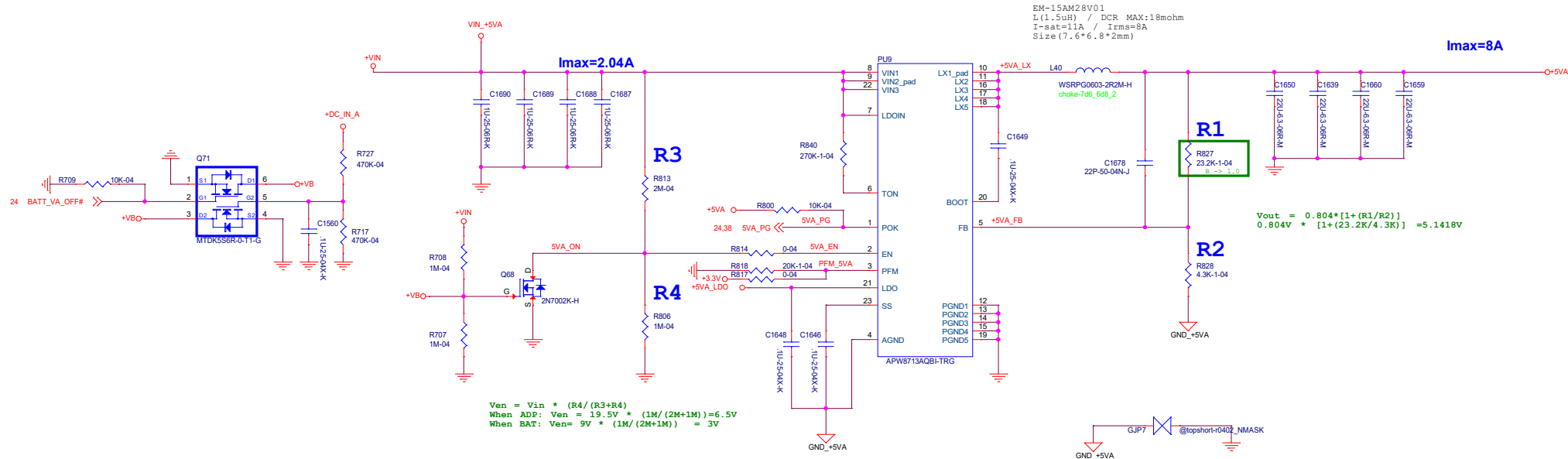


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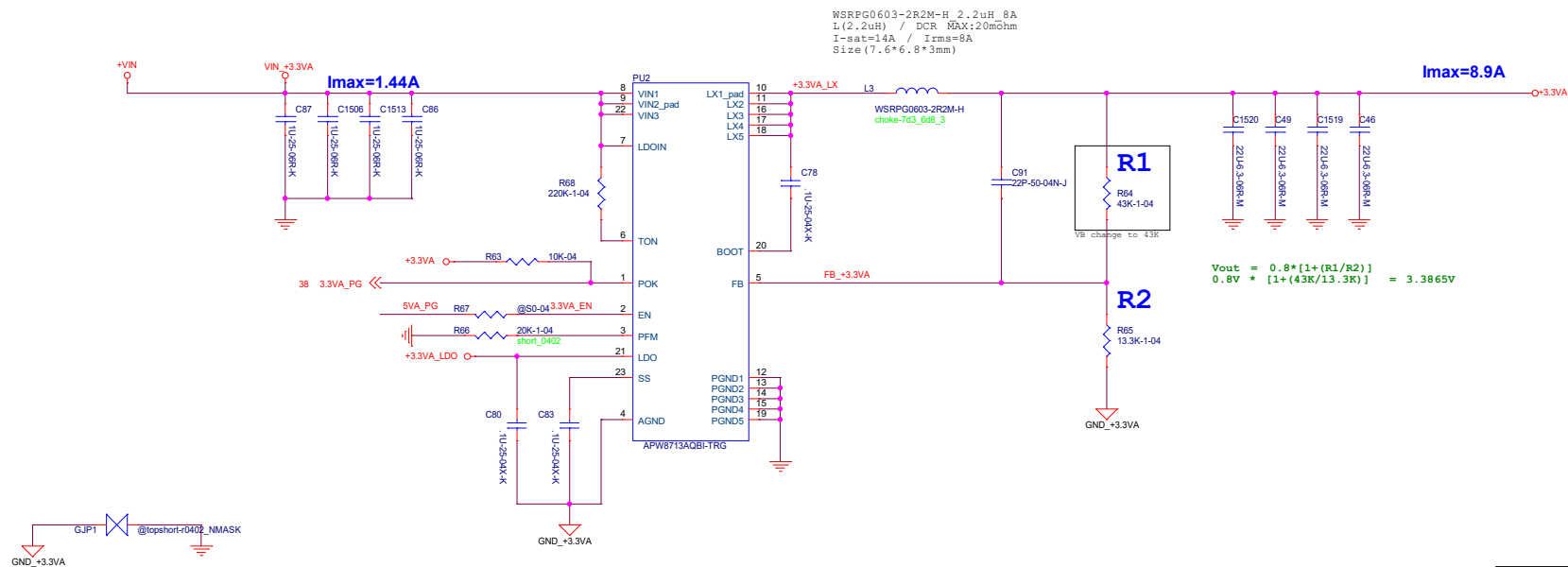
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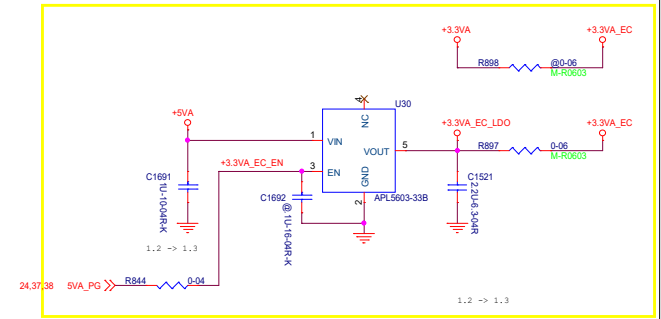
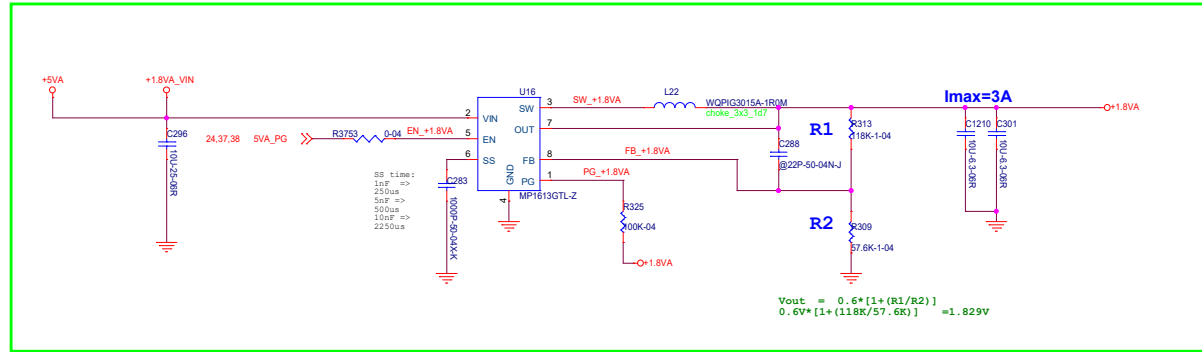
+5VA



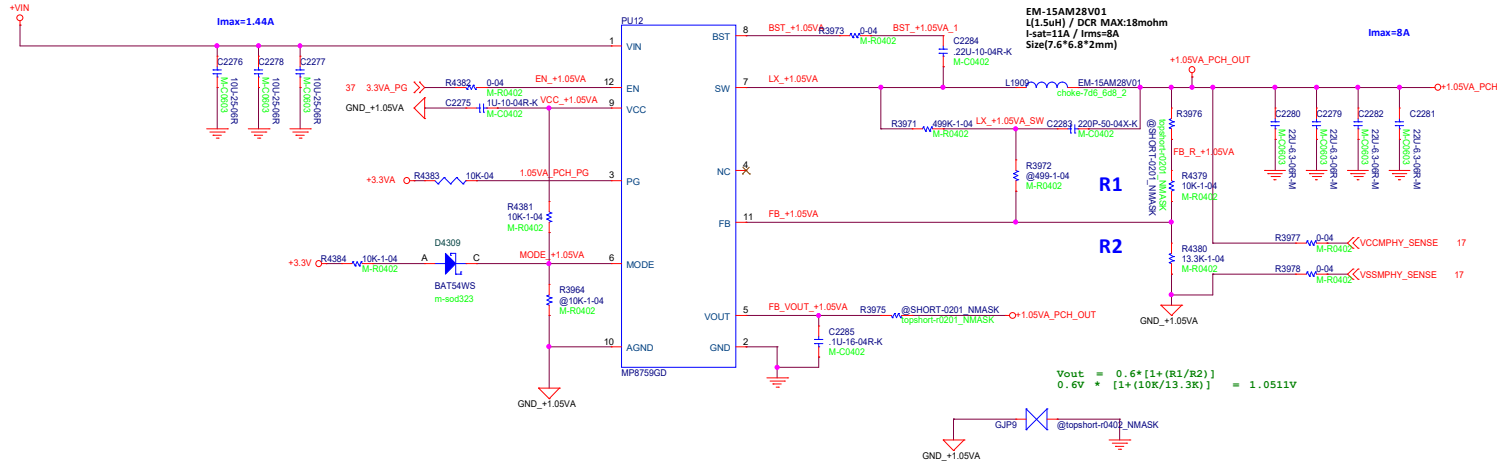
+3.3VA



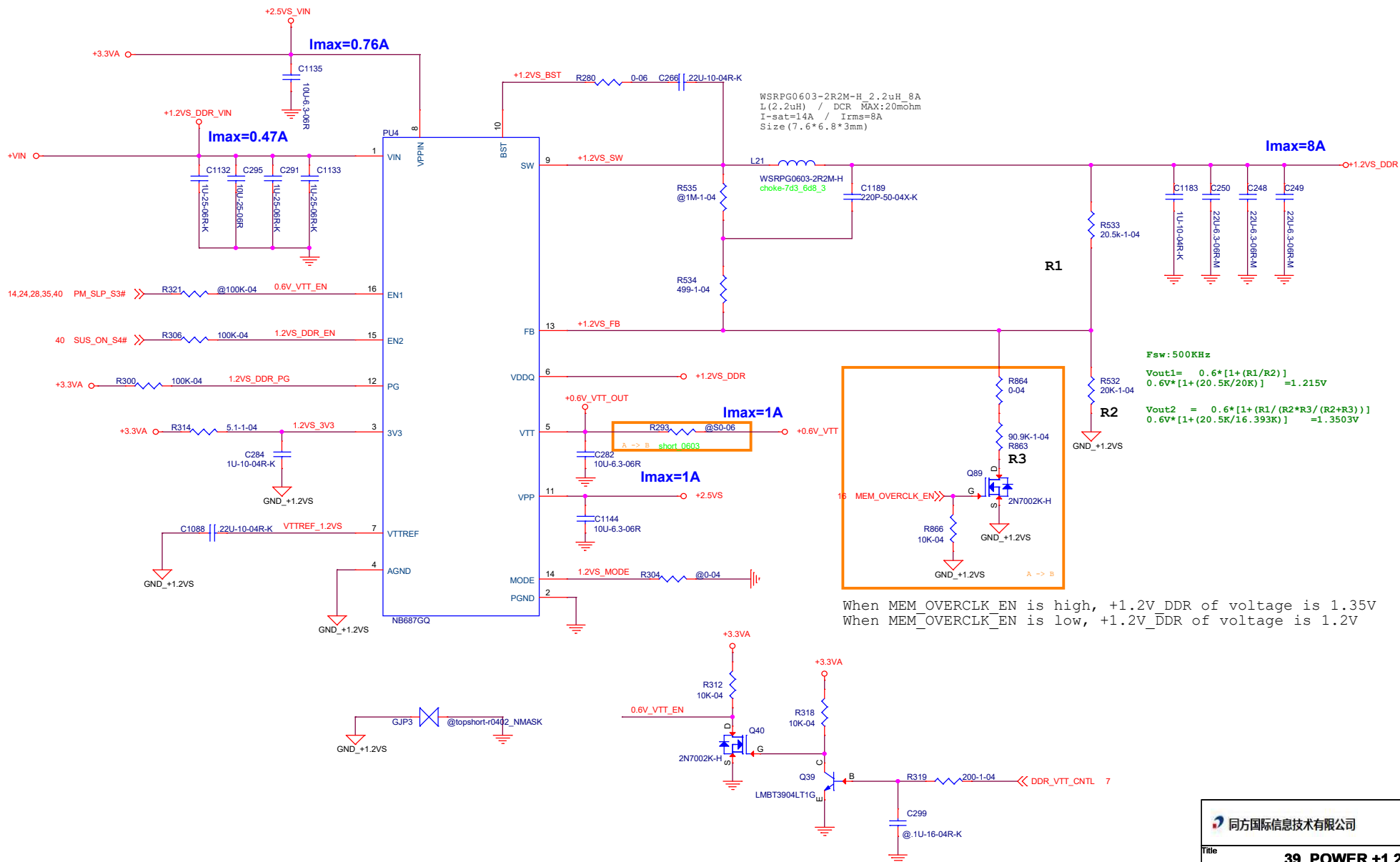
+3.3VA_EC



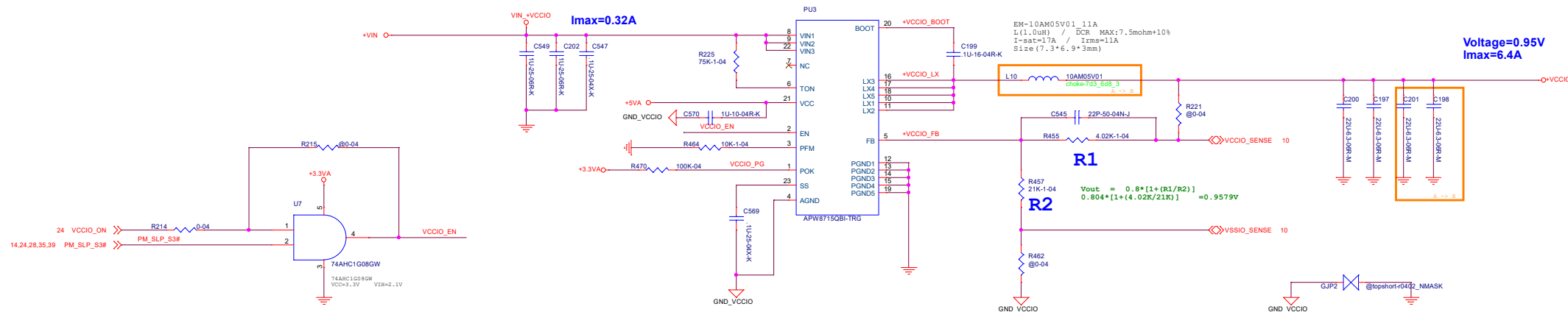
+1.05VA_PCH



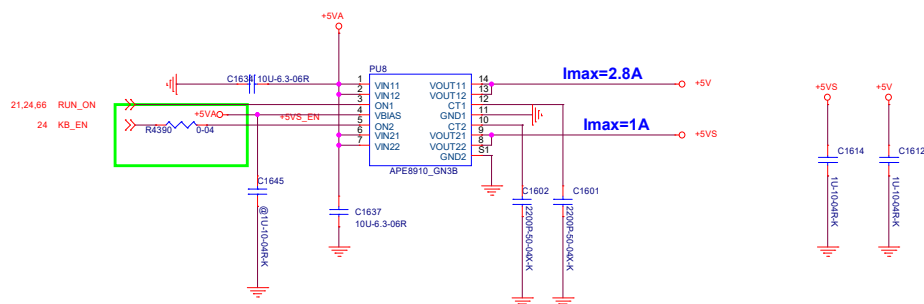
+1.2VS_DDR/+2.5VS/+0.6V_VTT



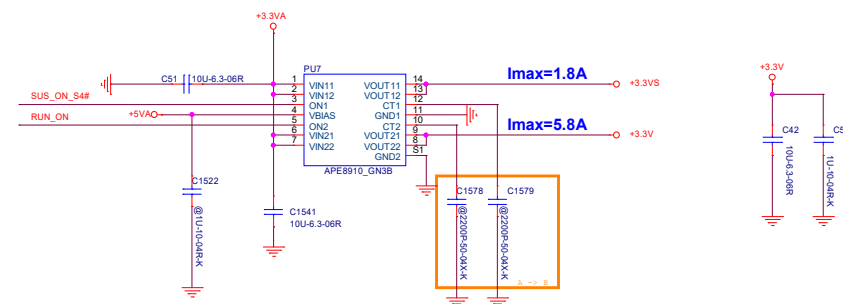
+VCCIO



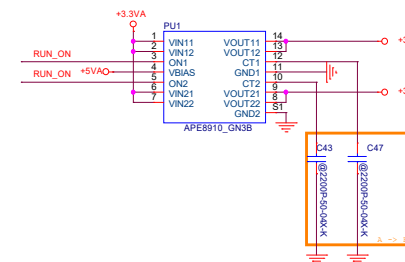
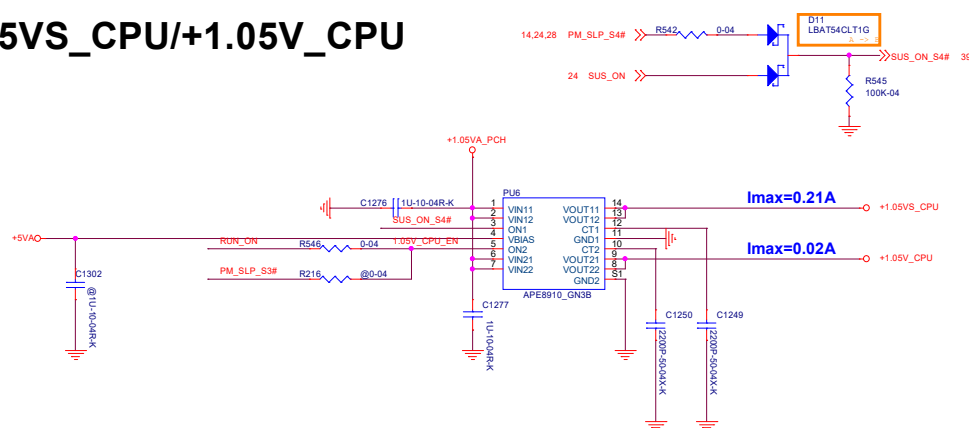
+5VS/+5V

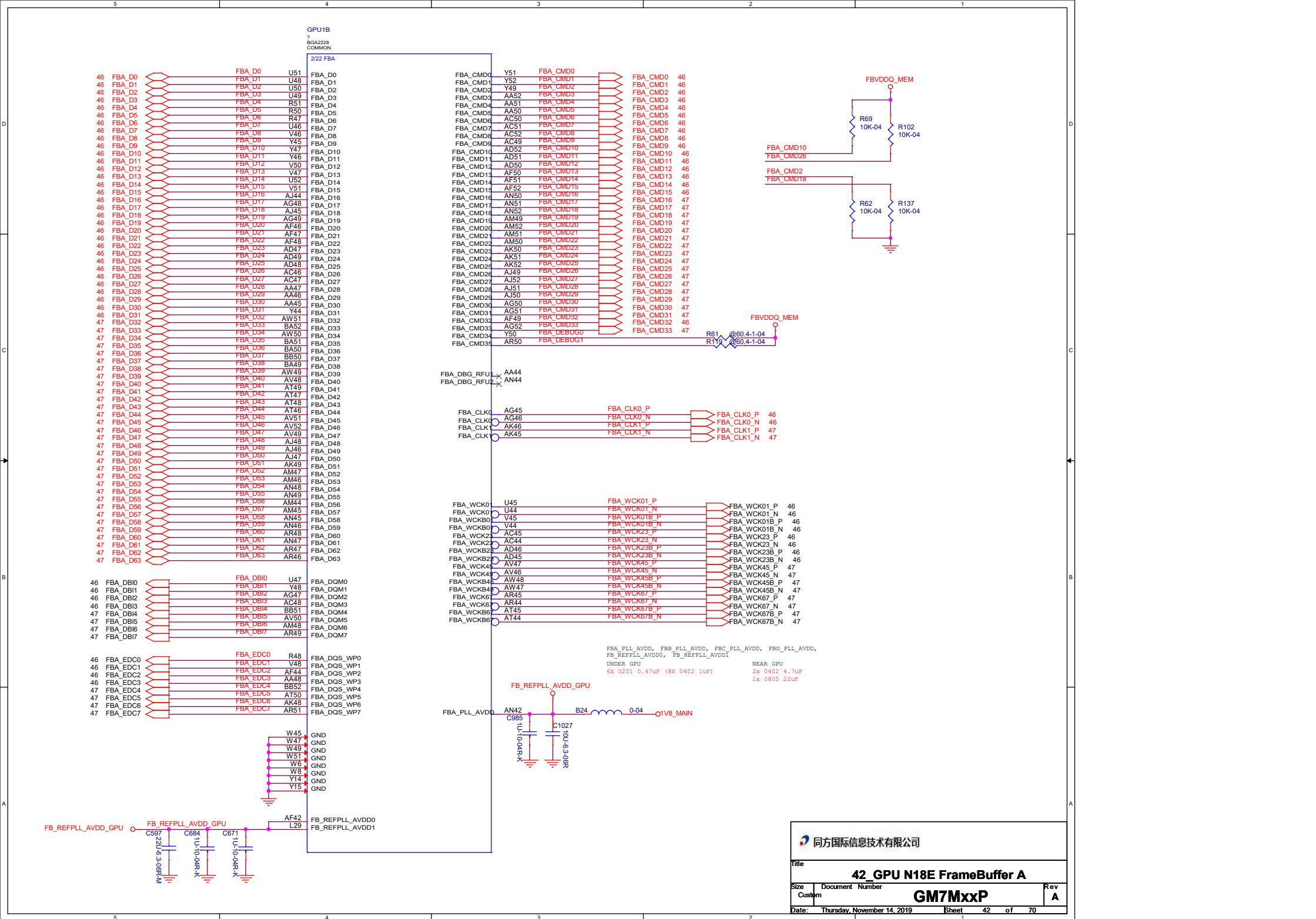


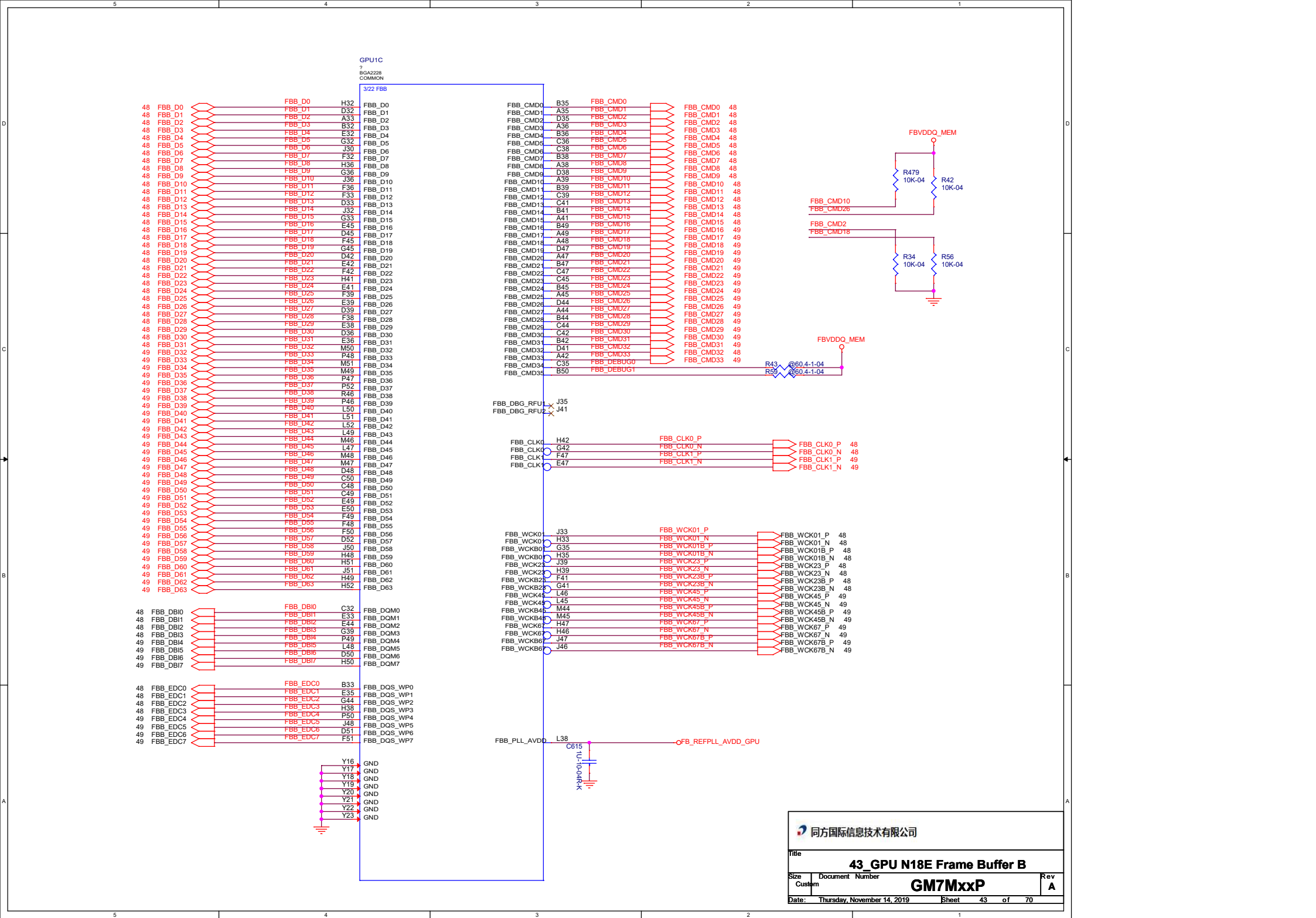
+3.3VS/+3.3V

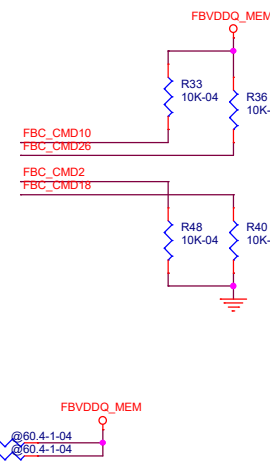


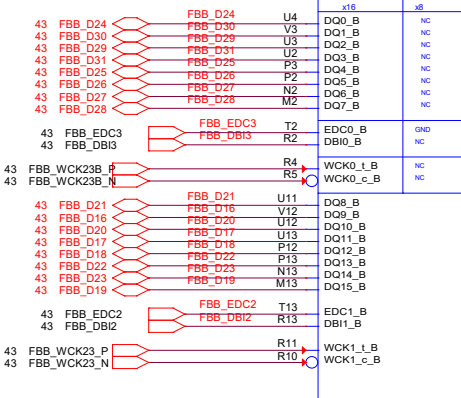
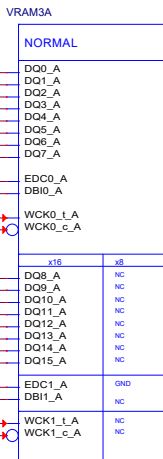
+1.05VS_CPU/+1.05V_CPU





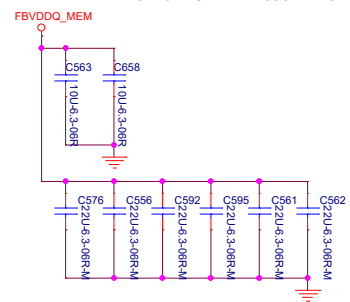
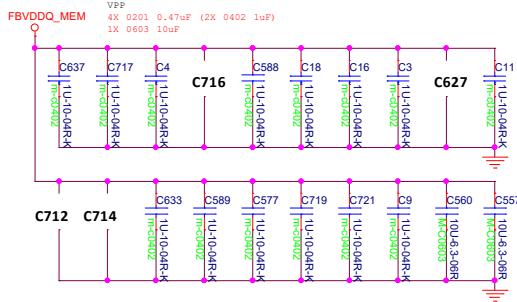
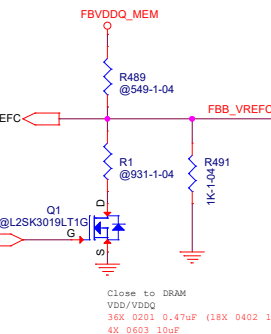
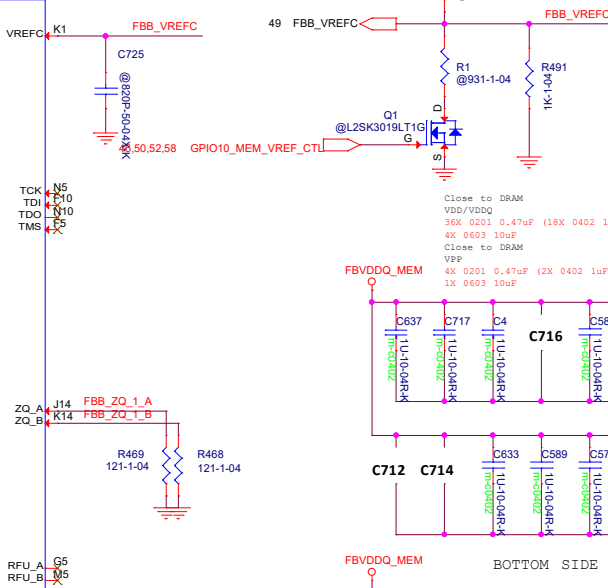
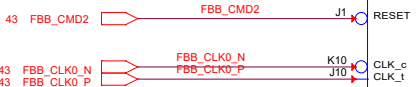
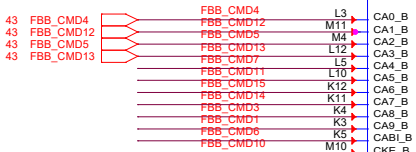
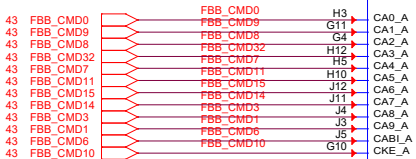
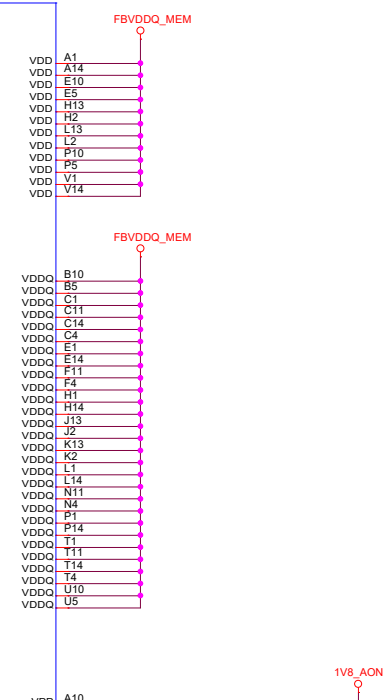
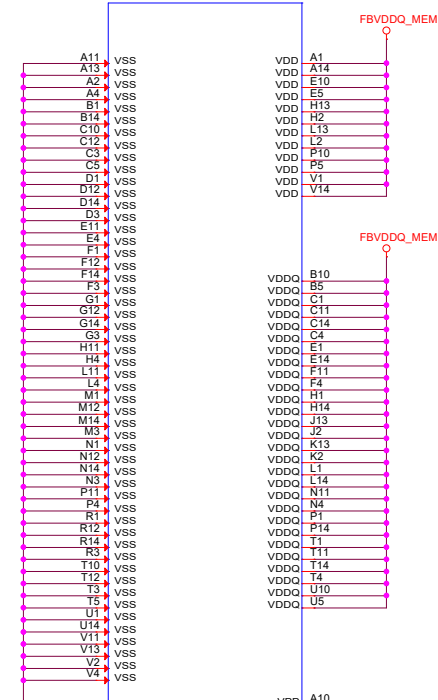




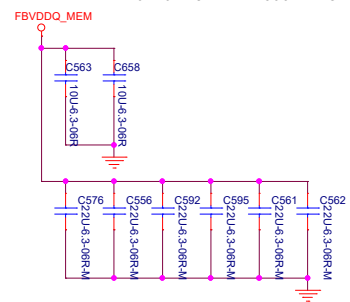


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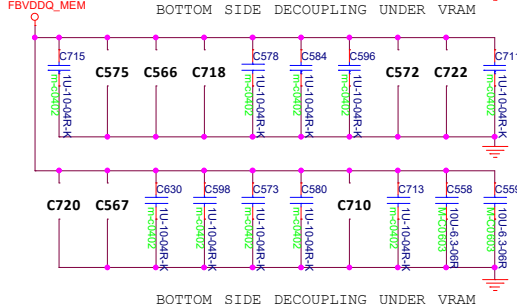
7
FBGA180
COMMON



BOTTOM SIDE DECOUPLING UNDER VRAM

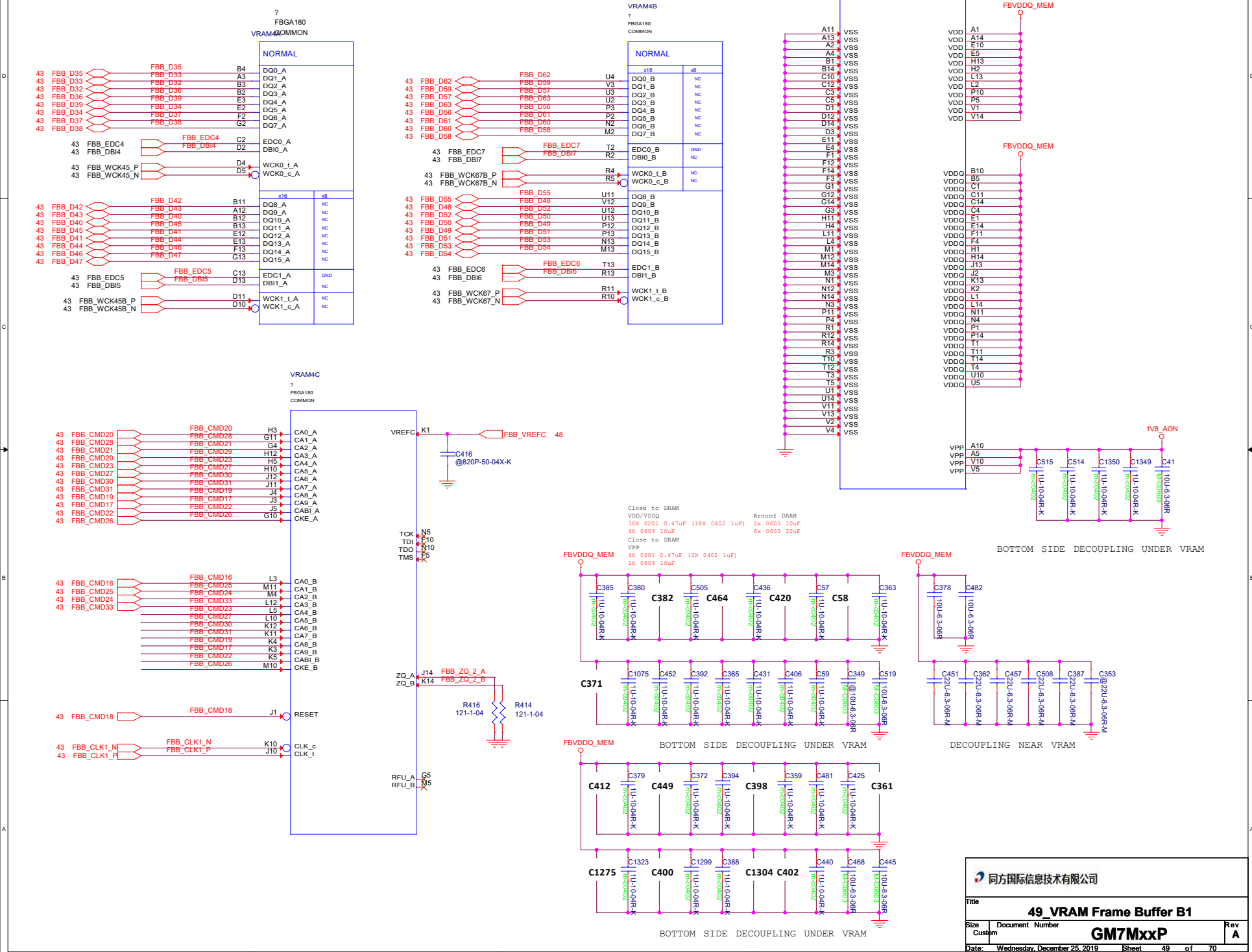


DECOUPLING NEAR VRAM

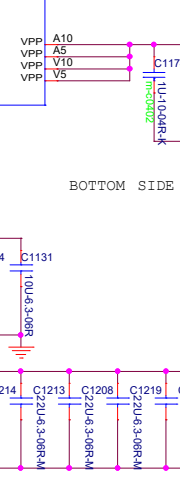
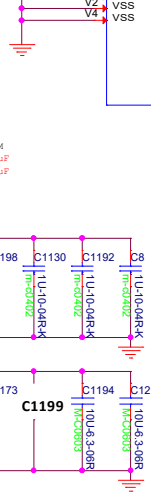
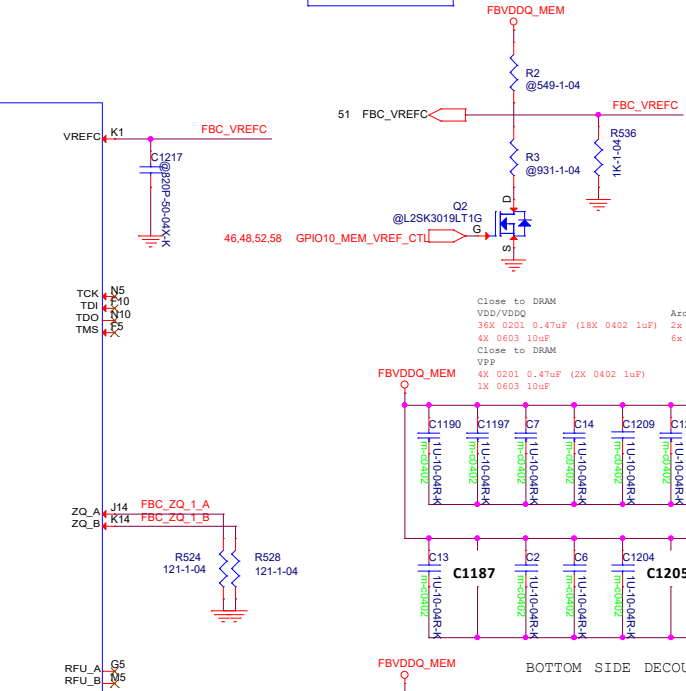
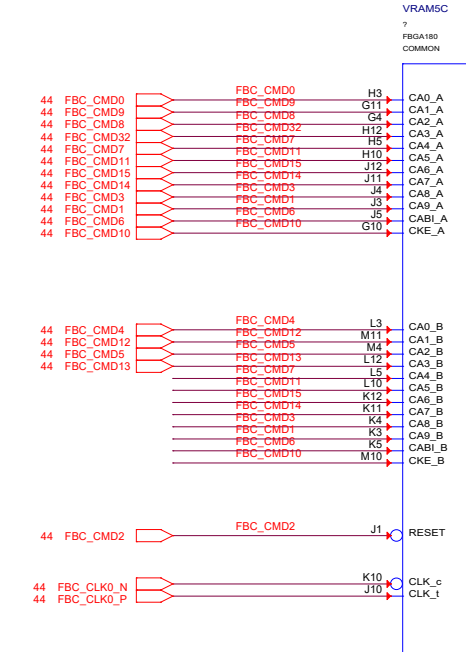
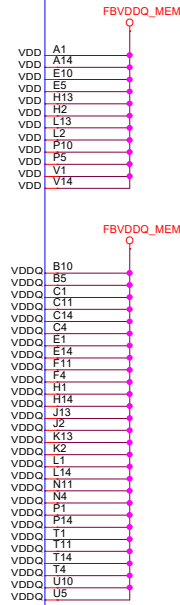
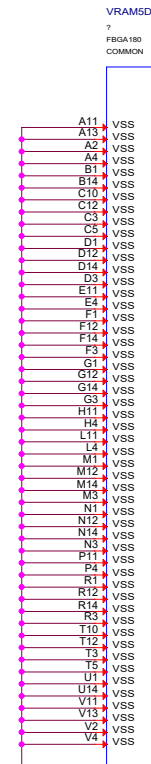
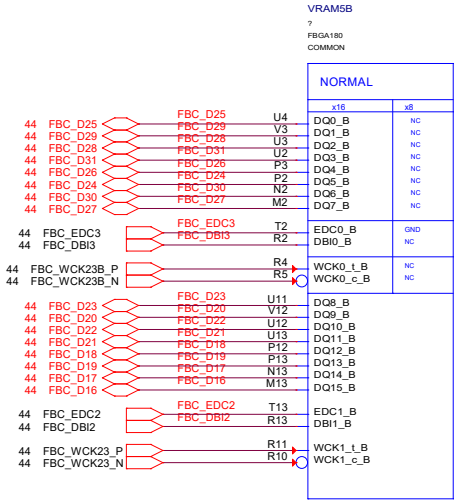
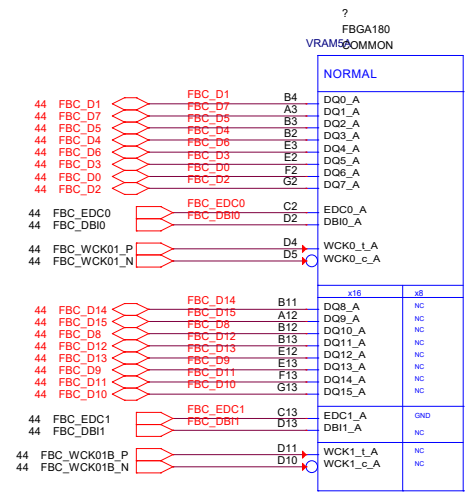


BOTTOM SIDE DECOUPLING UNDER VRAM

Maximum VRAM case Temp is 85 celcibus degree



MEM_FBC[31_0]



BOTTOM SIDE DECOUPLING UNDER VRAM

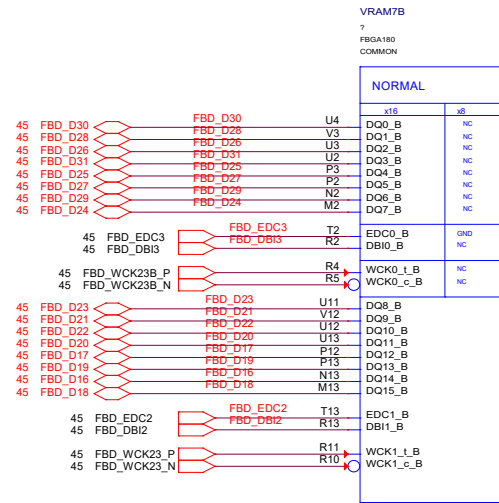
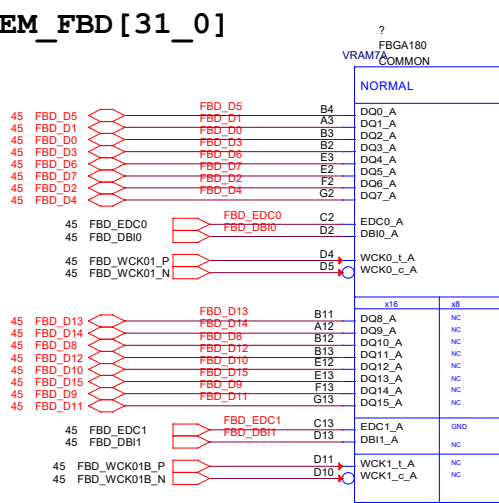
DECOUPLING NEAR VRAM

BOTTOM SIDE DECOUPLING UNDER VRAM

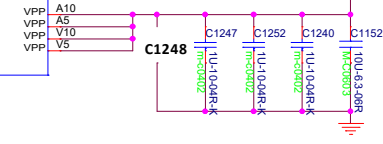
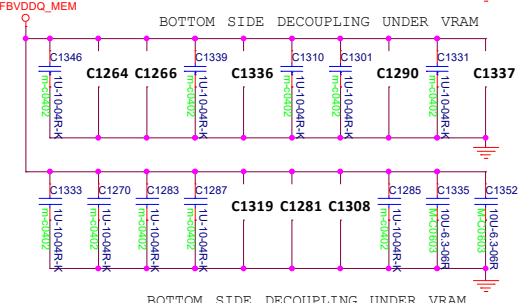
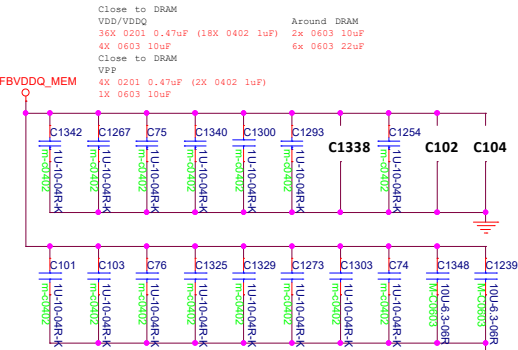
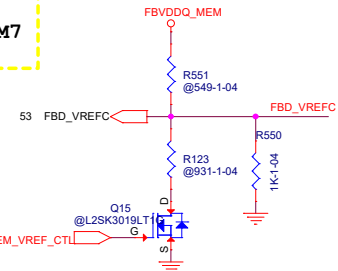
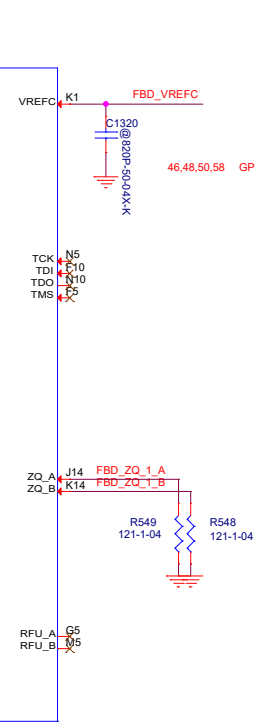
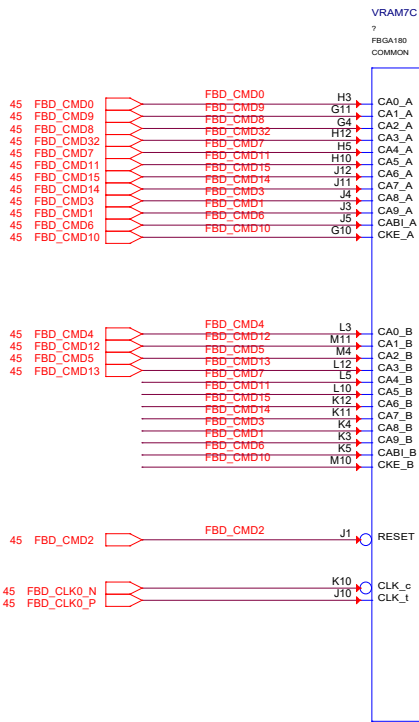
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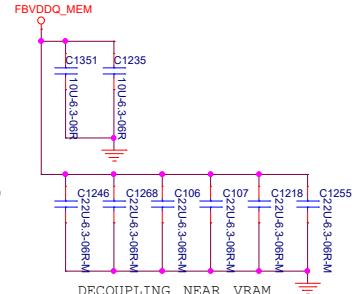
MEM_FBD[31_0]



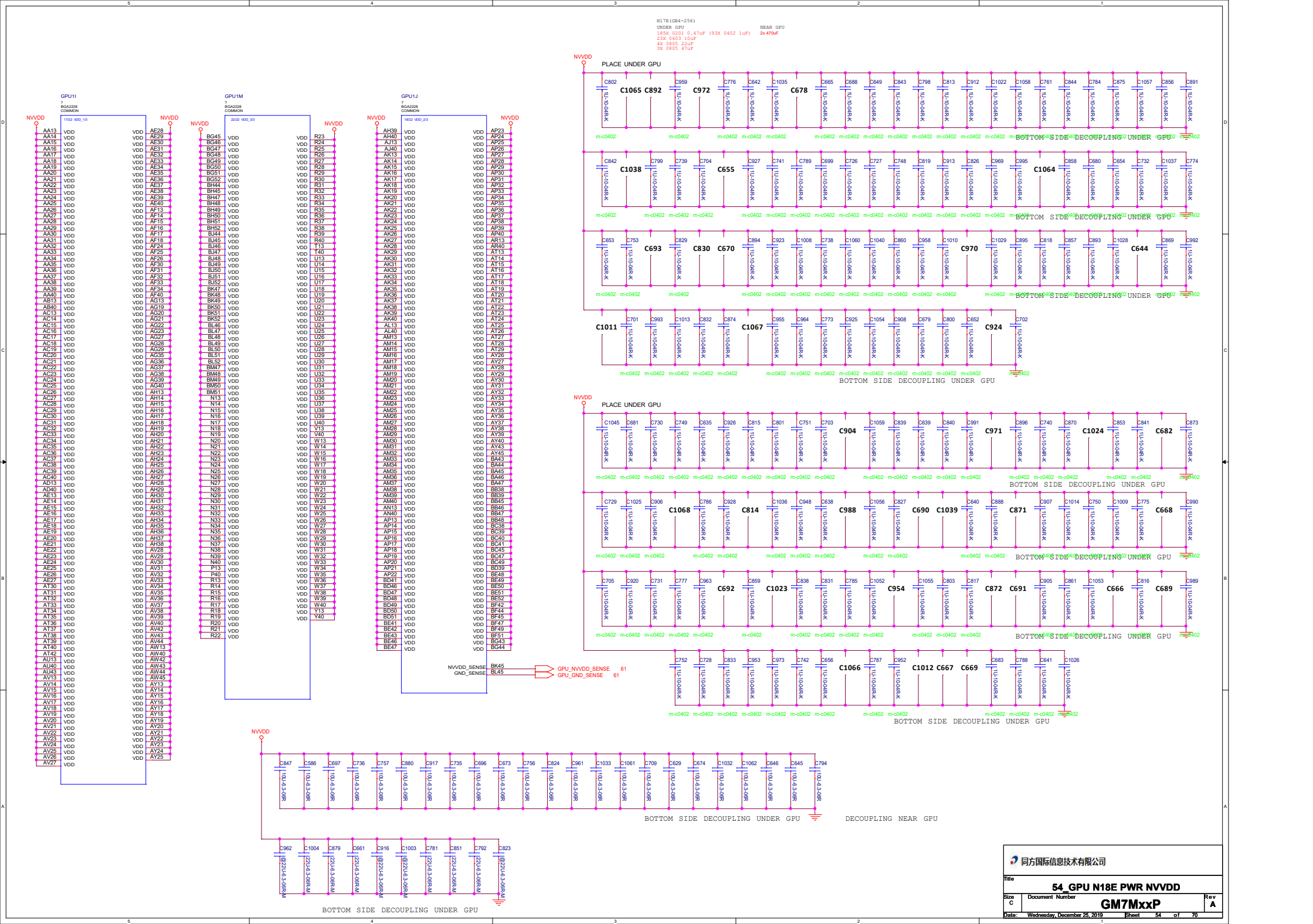
For N18E-G1 don't need to mount VRAM7



BOTTOM SIDE DECOUPLING UNDER VRAM



DECOUPLING NEAR VRAM





Hardware Design Guide Page282:
For IFPA/B/C/D/E/F
If an IFP link is not used, it should be NC
including power rail and signal and references
associated with LINKX

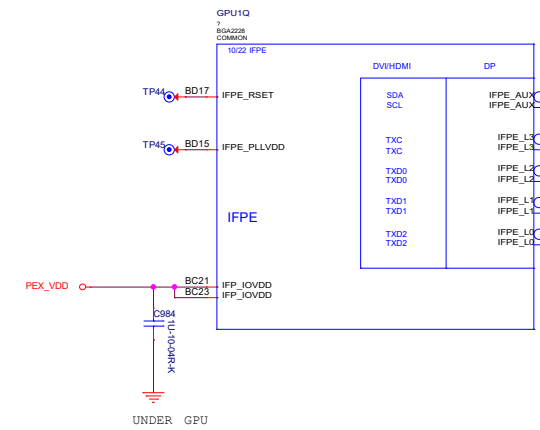
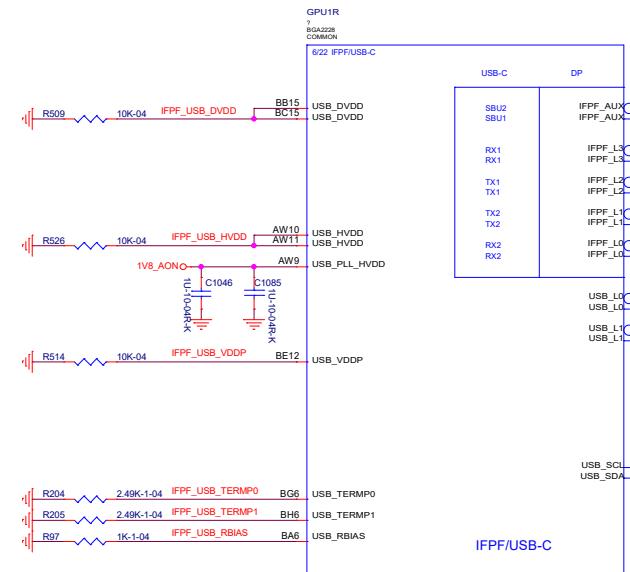
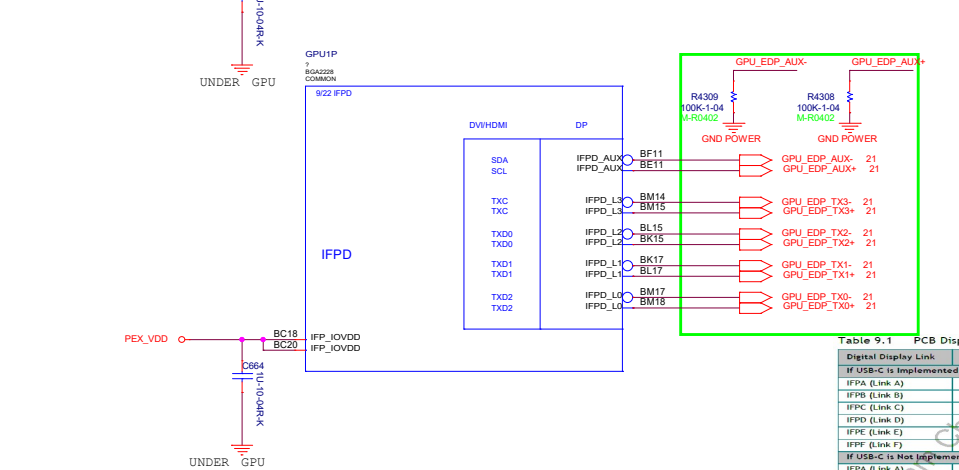
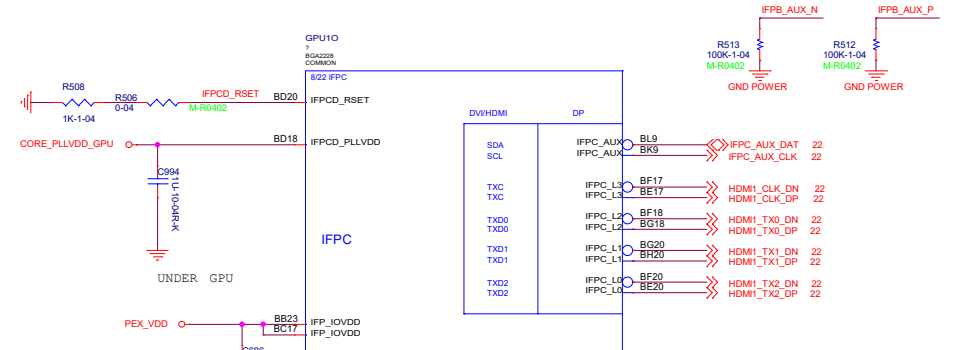
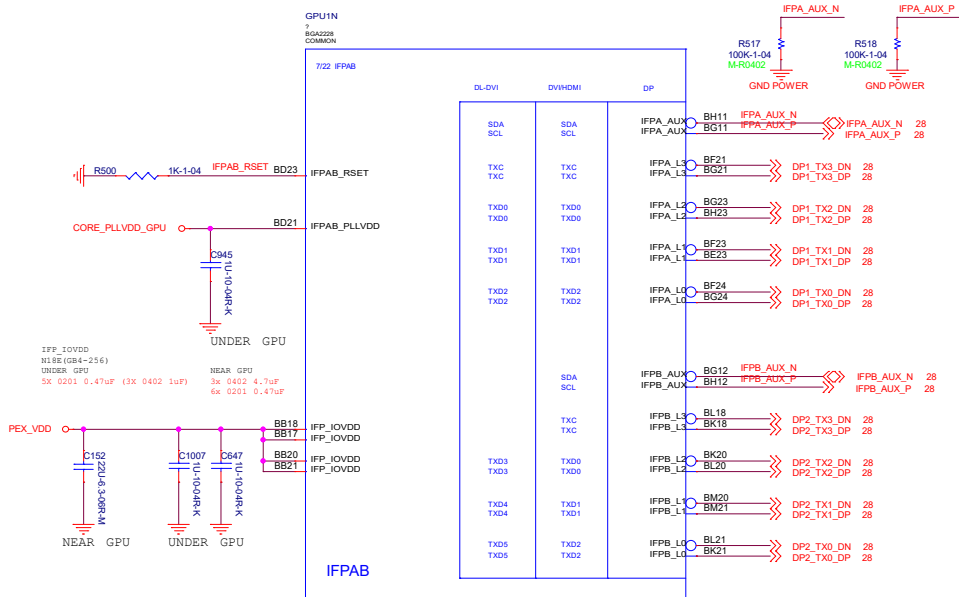
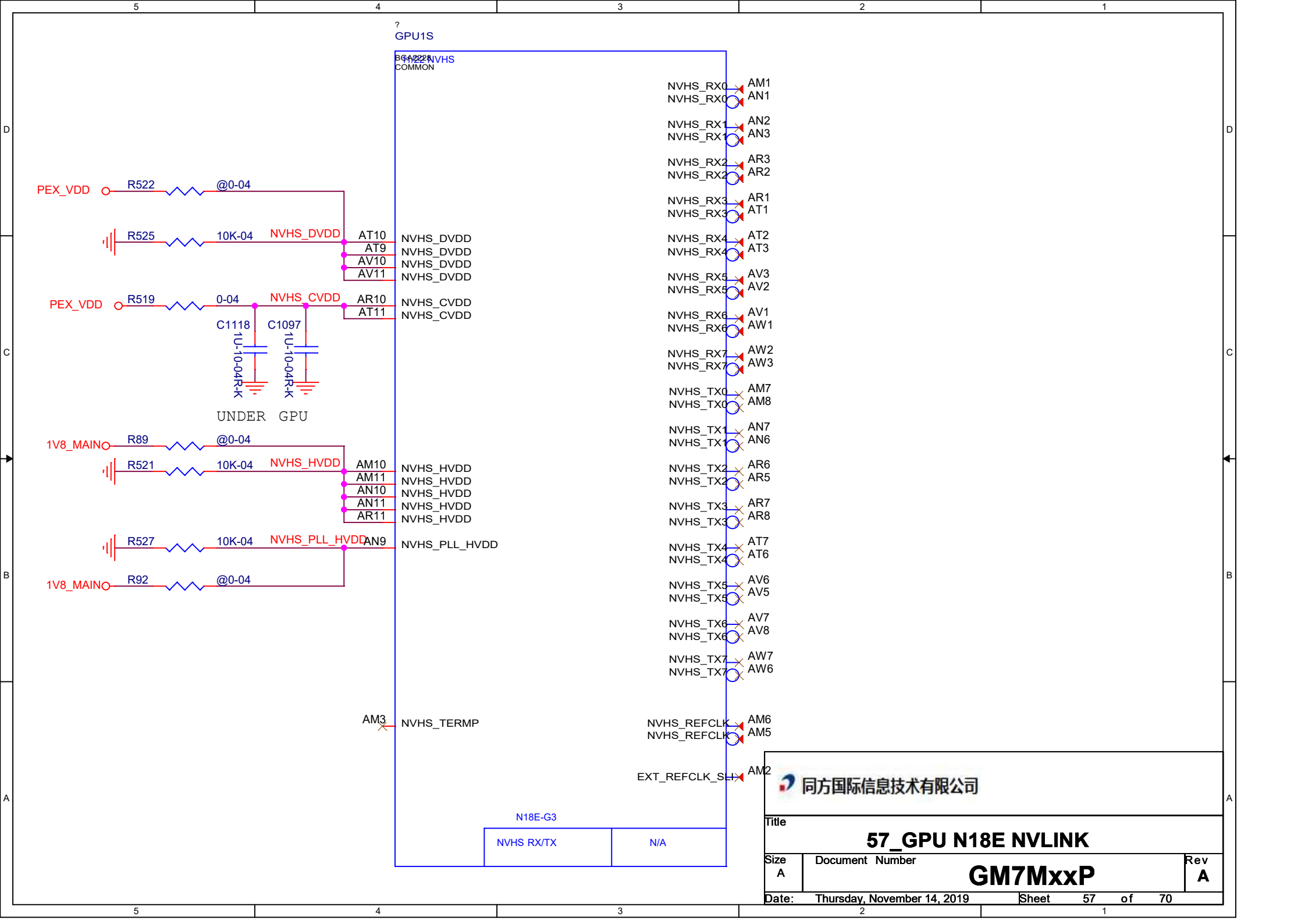
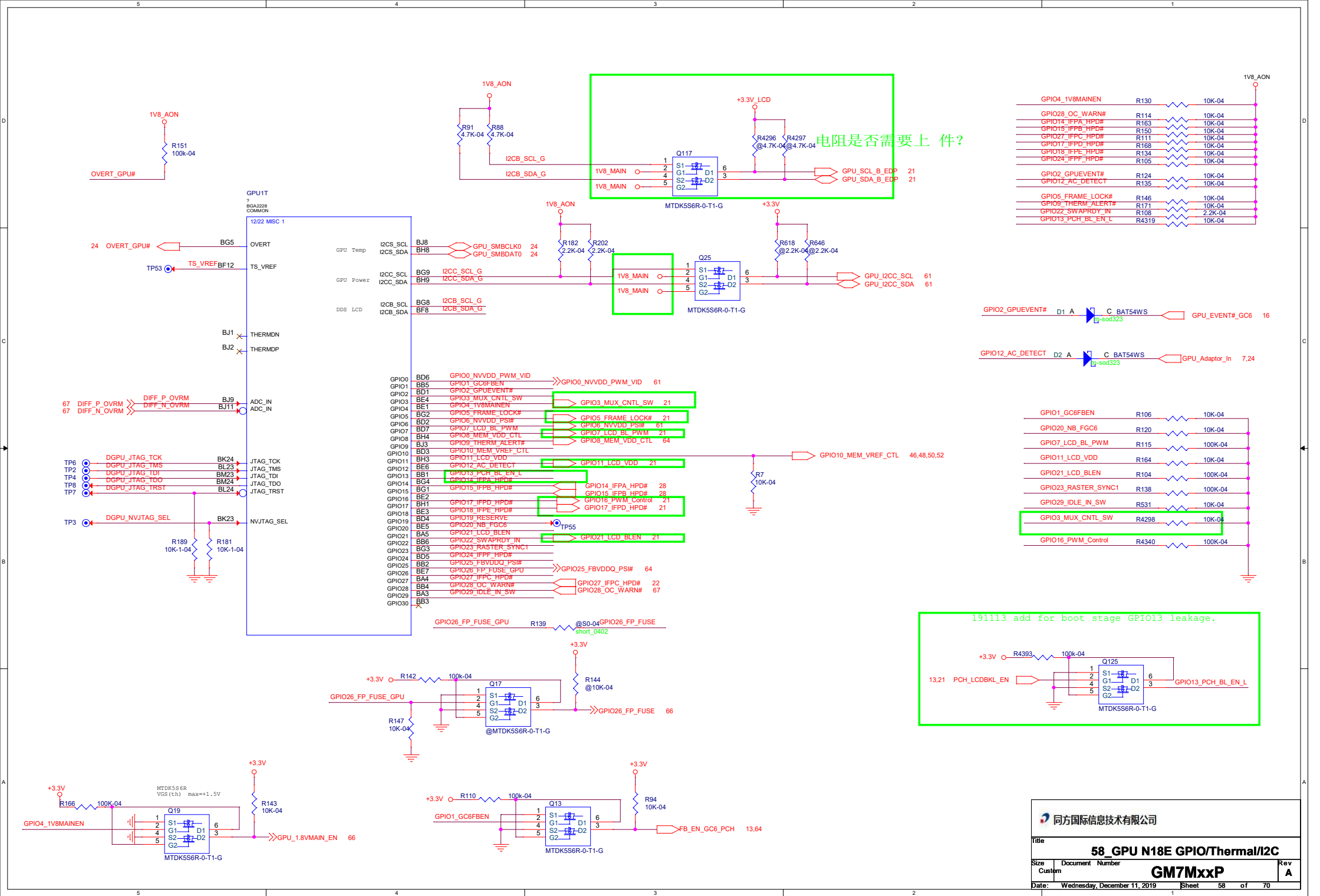
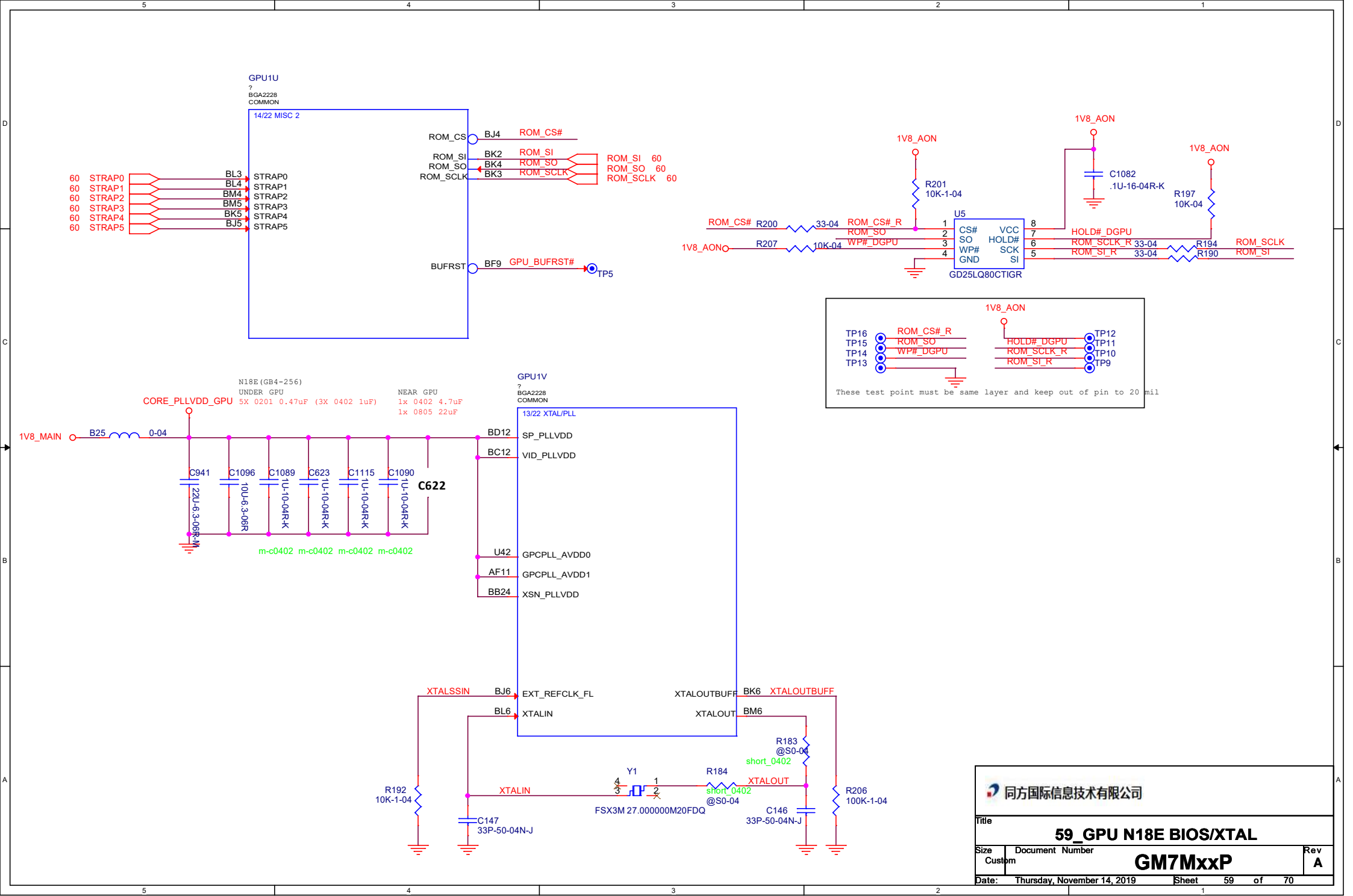


Table 9.1 PCB Display Link Summary (G848-256 packages)

Digital Display Link	Dual-Link DVI	HDMI	sDP	DisplayPort	USBC
If USB-C is implemented					
IFPA (Link A)	✓ (Dual Link with IFPB)			✓	
IFPB (Link B)	✓ (Dual Link with IFPA)				
IFPC (Link C)		✓		✓	
IFPD (Link D)			✓	✓	
IFPE (Link E)					✓
IFPF (Link F)					
If USB-C is Not implemented					
IFPA (Link A)	✓ (Dual Link with IFPB)			✓	
IFPB (Link B)	✓ (Dual Link with IFPA)				
IFPC (Link C)		✓		✓	
IFPD (Link D)			✓	✓	
IFPE (Link E)					✓
IFPF (Link F)					







LEVEL	Voltage (V)		
	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

Table 11.4 FS_OVERT* Strap Enablement

Strap Pins see Note			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note that configurations other than the two listed in Table 11.4 must be avoided, as otherwise damage to strap inputs may result.

For N18x GPUs the hardware (on-PCB) SOR_EXPOSED straps are redacted; ROM_SO, ROM_SI and ROM_SCLK straps are no longer provided. The register-based method for configuring audio for display links is the only method provided. This method is implemented in VBIOS settings.

Based on RVL_07916_001_V10 JUNE 2017

GDDR5				Strap	Strap 2	Strap 1	Strap 0
Density	Vendor	Part Number					
8Gb	Samsung	K4Z80325BC-HC14 C-die	0X0	L	L	L	
8Gb	Micron	MT61K256M32JE-14:A A-die	0X1	L	L	H	
8Gb	Hynix	H56C8H24MJR-S4C M-die	0X2	L	H	L	
4Gb	Samsung		0X7	H	H	H	
4Gb	Hynix		0X6	H	H	L	
4Gb	Micron						

POWER

1.25V/1.35V
1.25V/1.35V
1.25V/1.35V N18E-G2 only

			STRAP2		STRAP1		STRAP0	
			H	L	H	L	H	L
			R175	R188	R178	R176	R179	R177
Samsung	0x0	K4Z80325BC-HC14		V		V		V
Micron	0x1	MT61K256M32JE-14:A		V		V	V	

59 STRAP0
59 STRAP1
59 STRAP2
59 STRAP3
59 STRAP4
59 STRAP5

Strap5,4,3 LLH

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

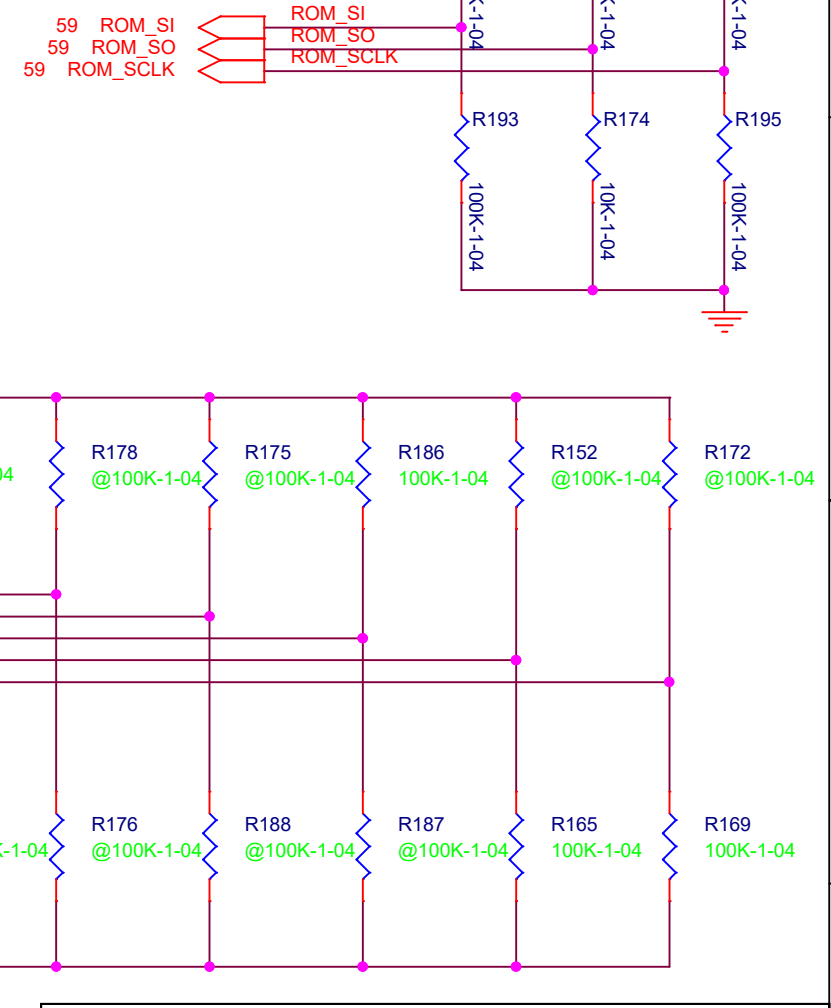
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

► **SMB_ALT_ADDR Enable:** This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits.

► **DEVID_SEL:** NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').

► **PCIE_CFG:** This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N18x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)

► **VGA_DEVICE:** This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits (consult NVIDIA for details on proper bit setting for MS-Hybrid solutions).



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Title

60_GPU N18E STRAP

Size A

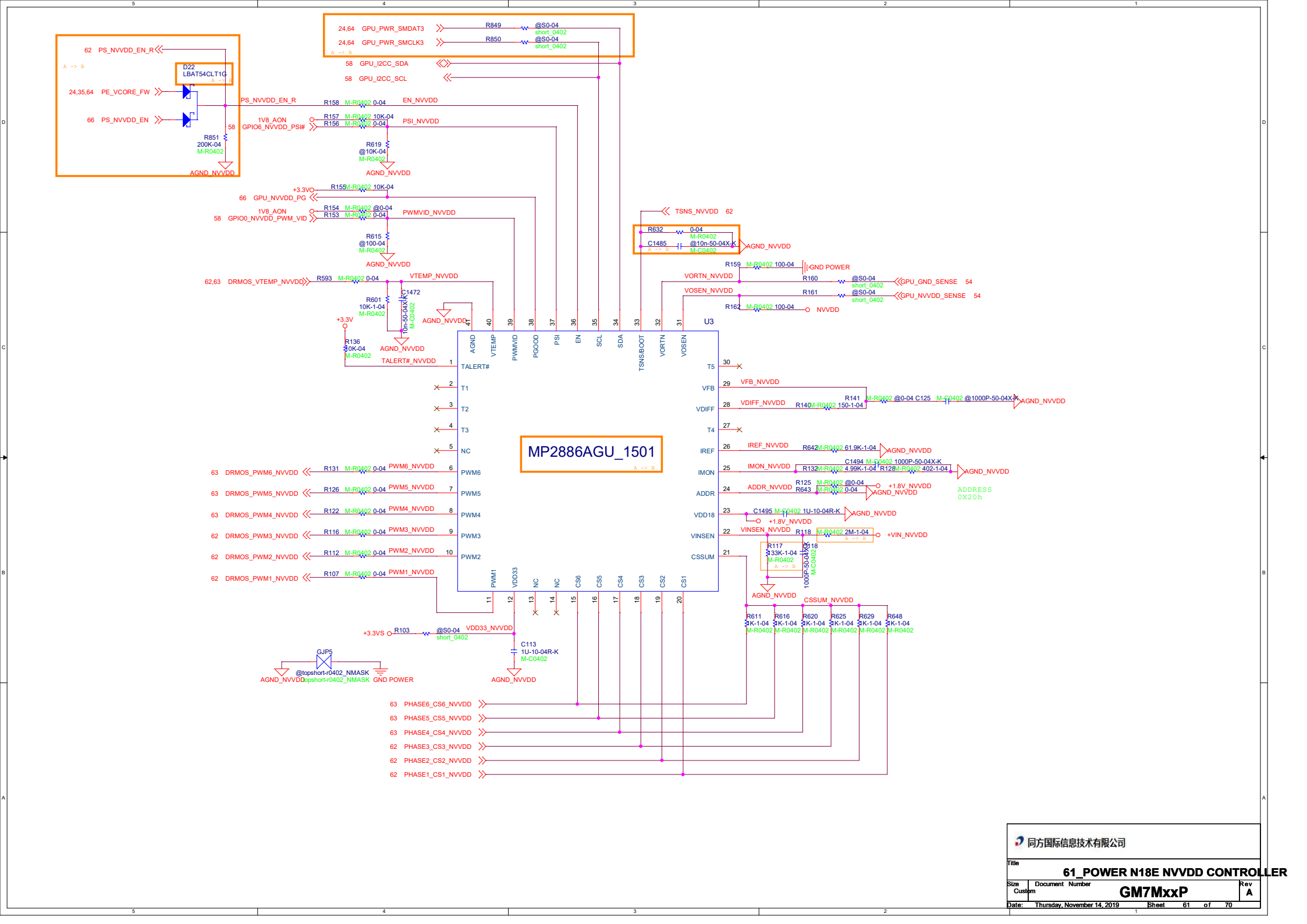
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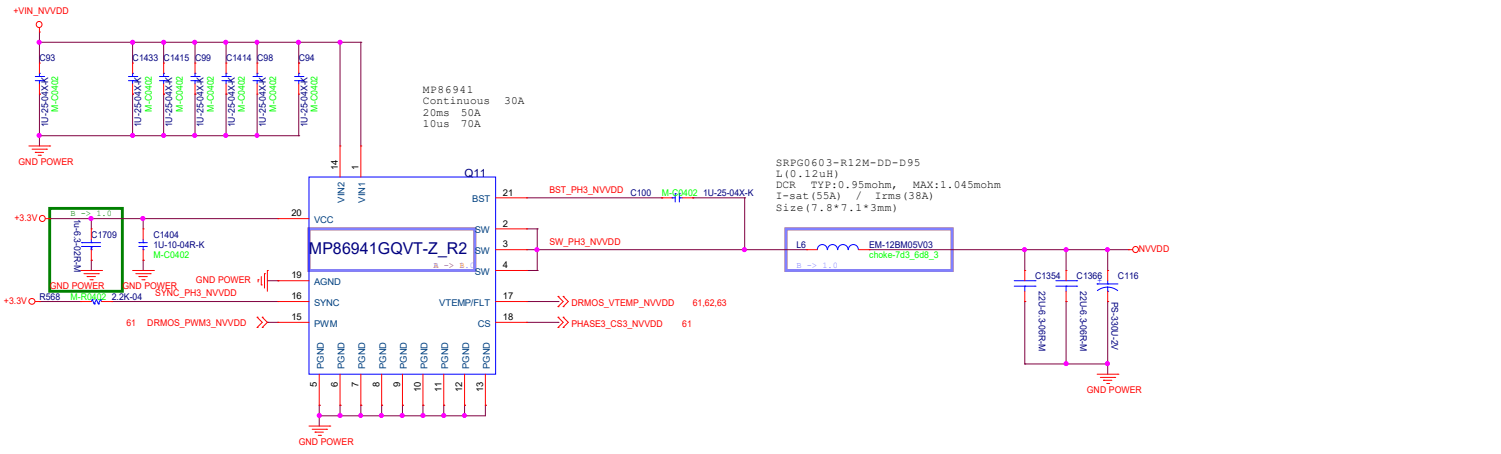
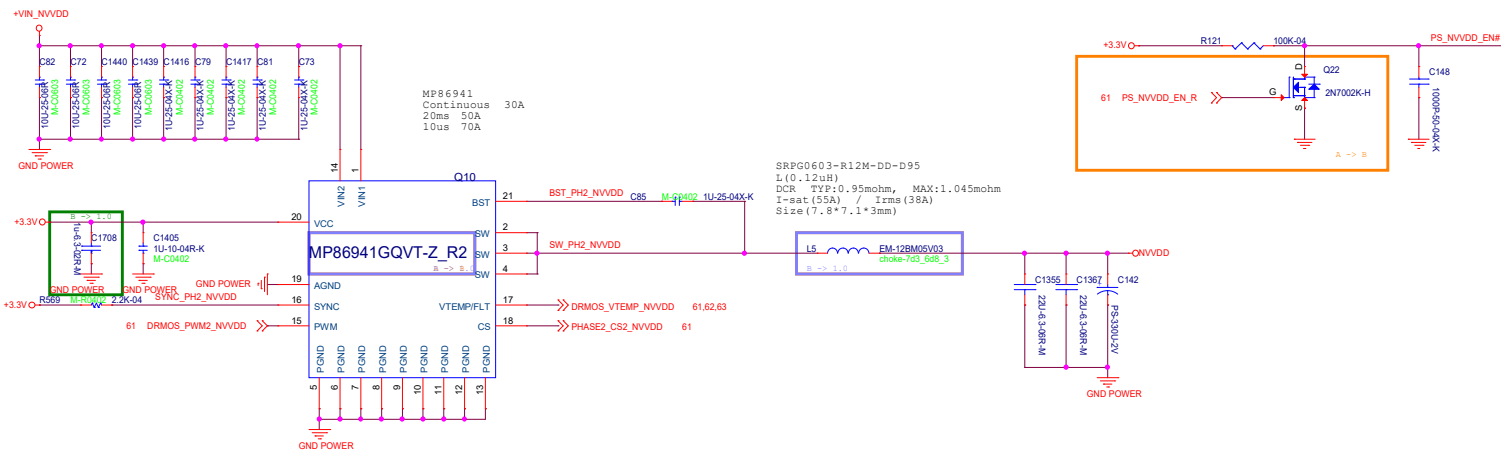
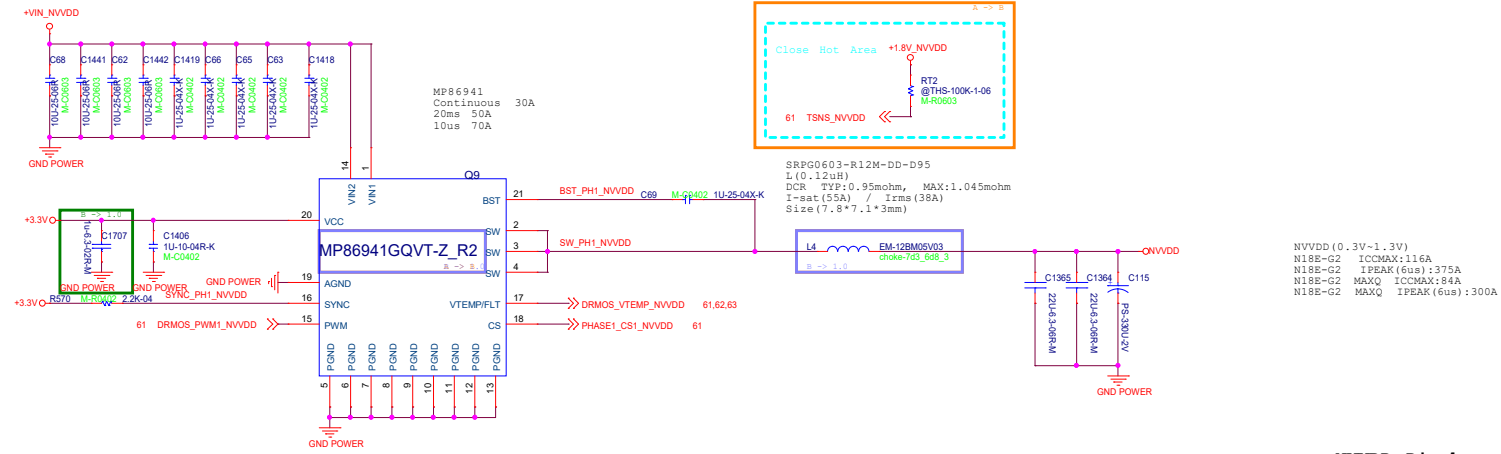
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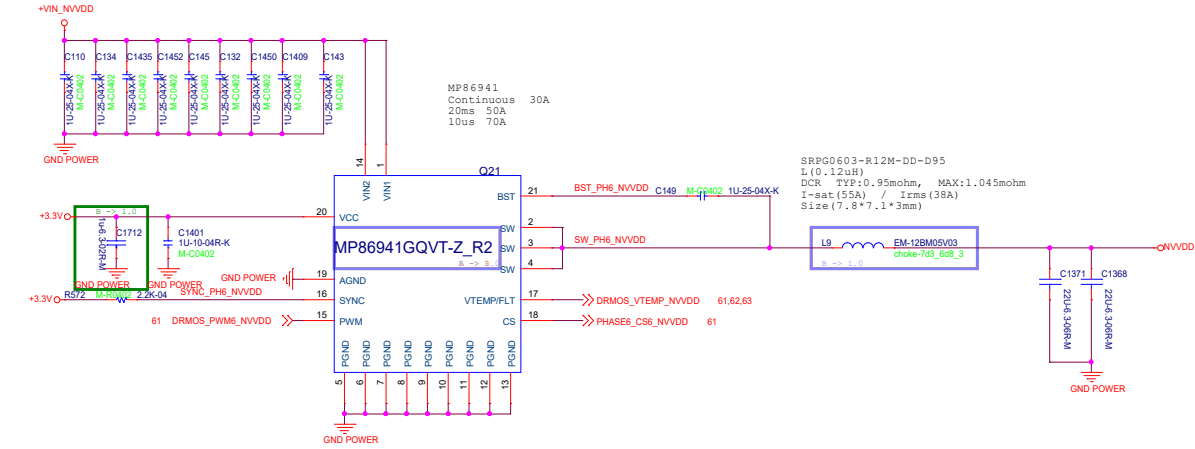
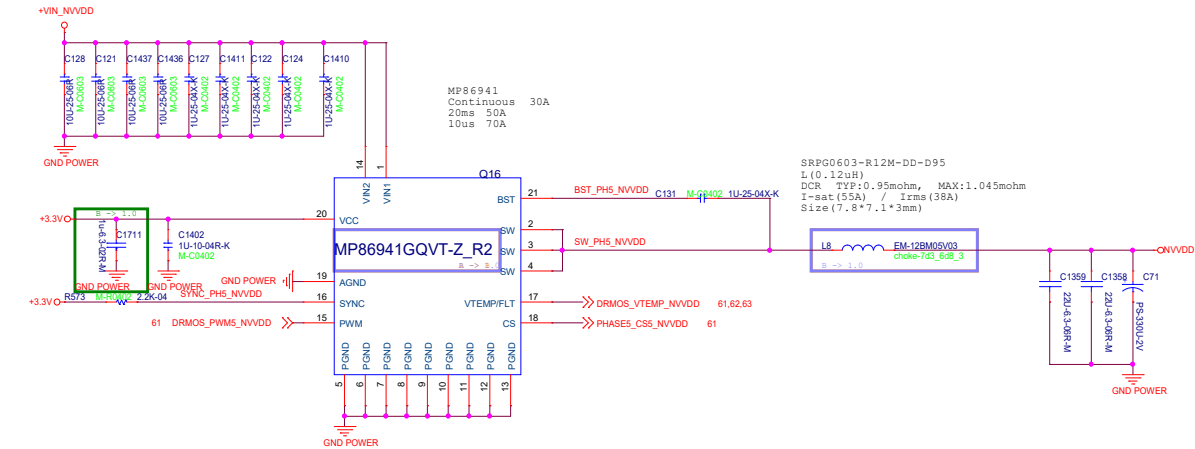
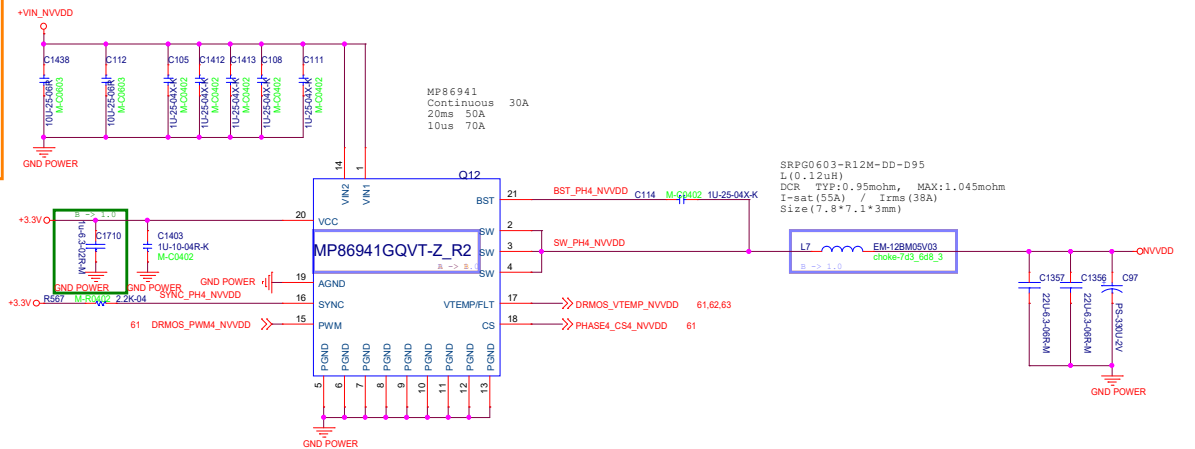
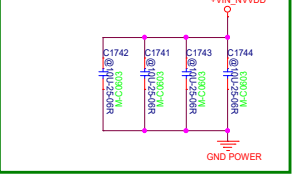
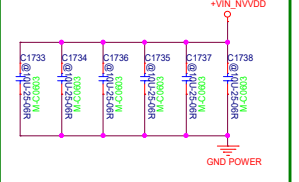
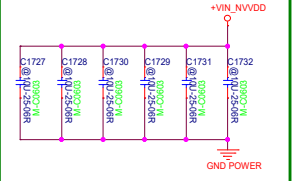
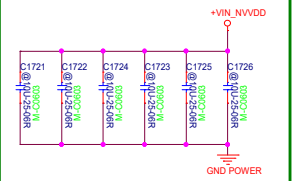
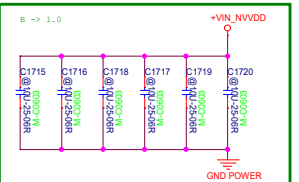
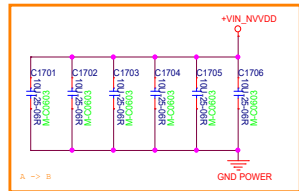
Rev A

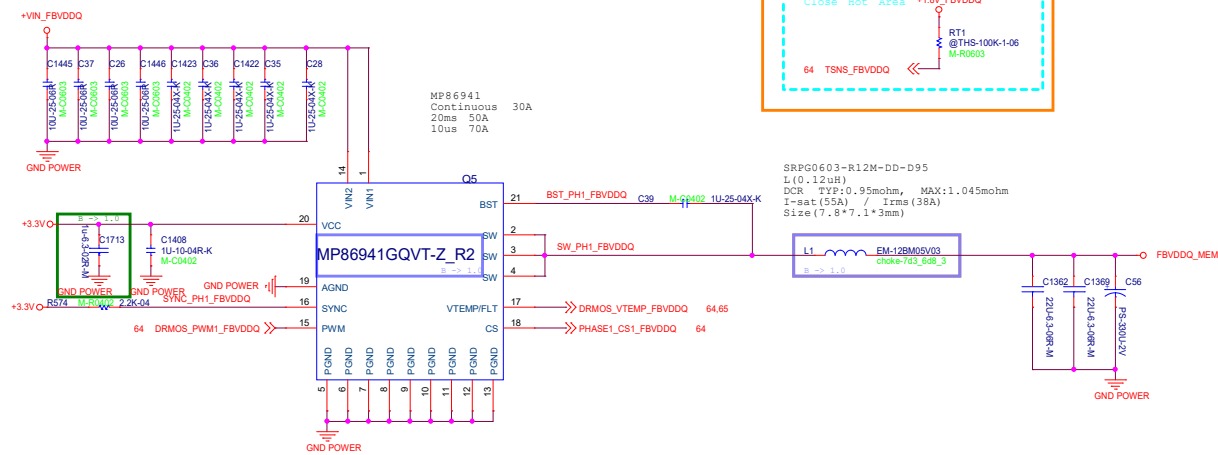
Date: Tuesday, November 19, 2019

Sheet 60 of 70

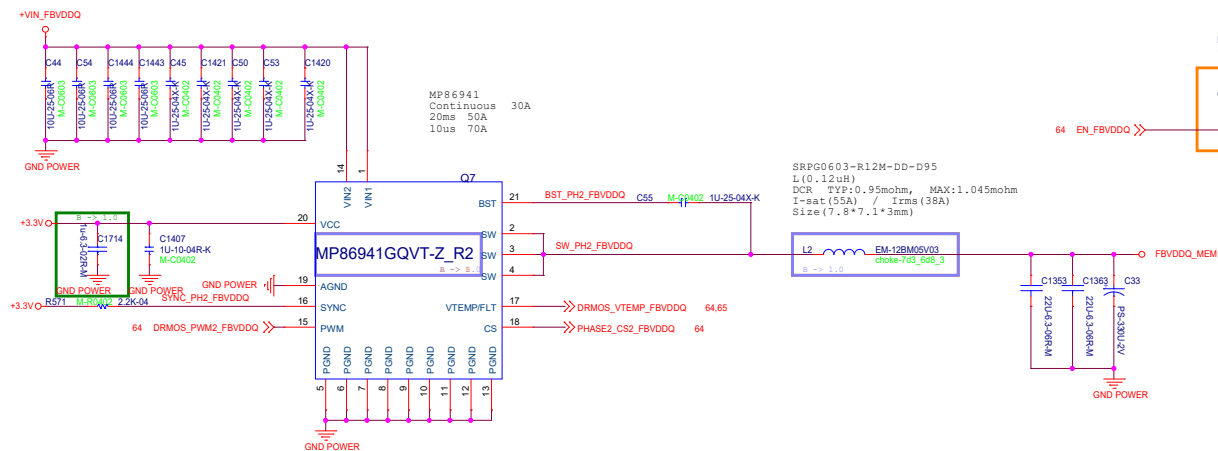




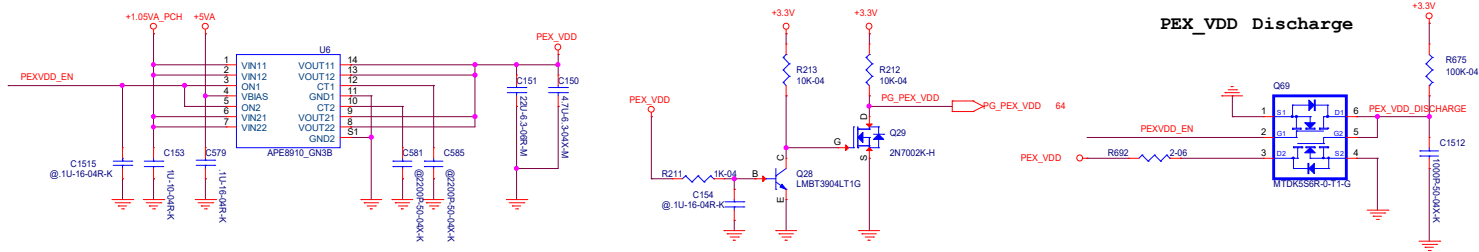




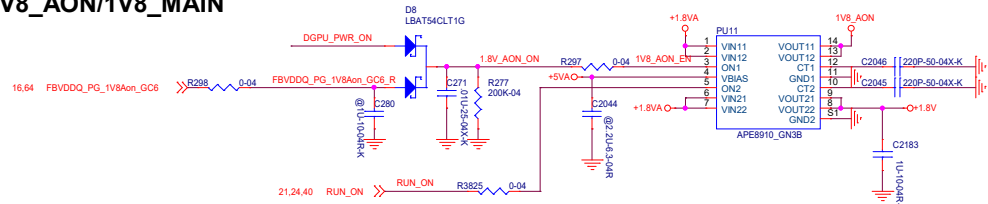
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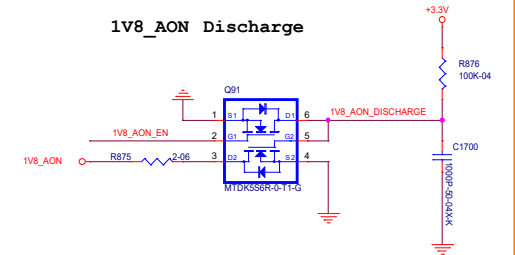
PEX_VDD SW



1V8_AON/1V8_MAIN

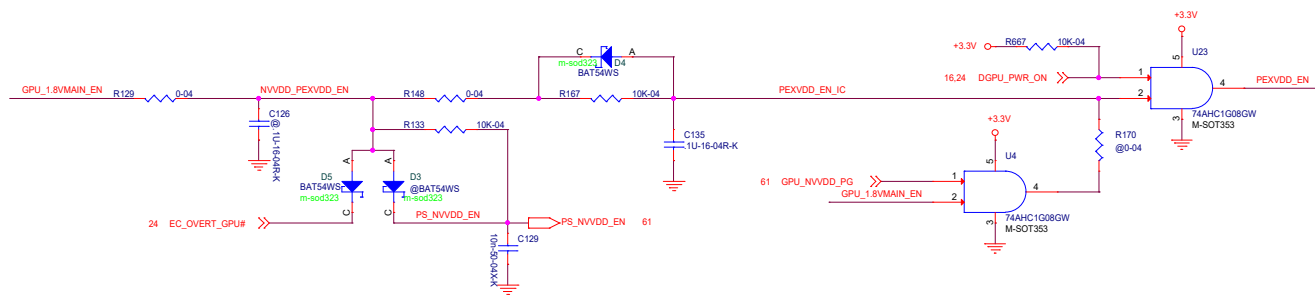
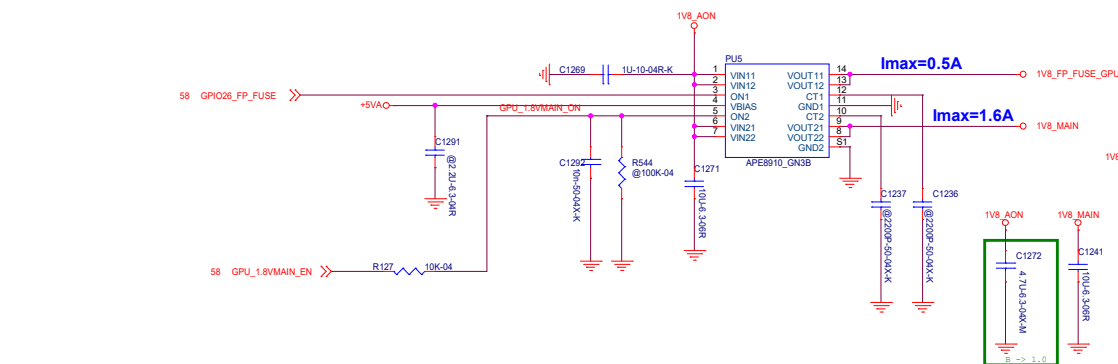
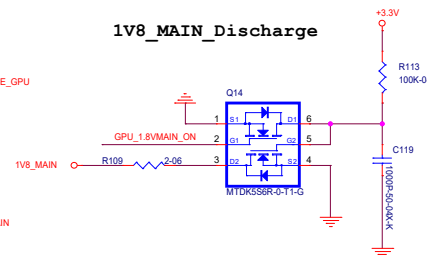


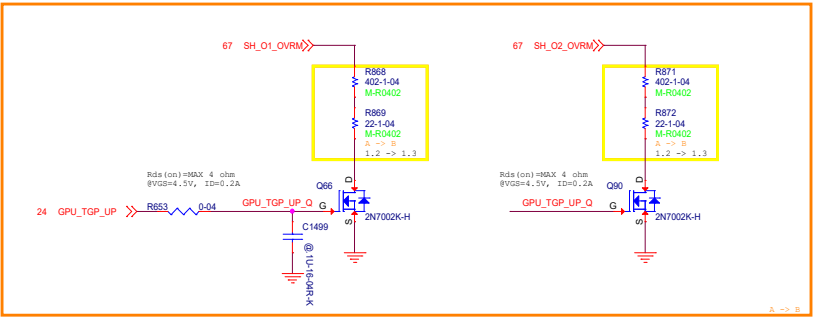
1V8_AON Discharge



$$V_{out} = \frac{0.6V \cdot [1 + (R1/R2)]}{[1 + (118K/57.6K)]} = 1.829V$$

1V8 MAIN Discharge



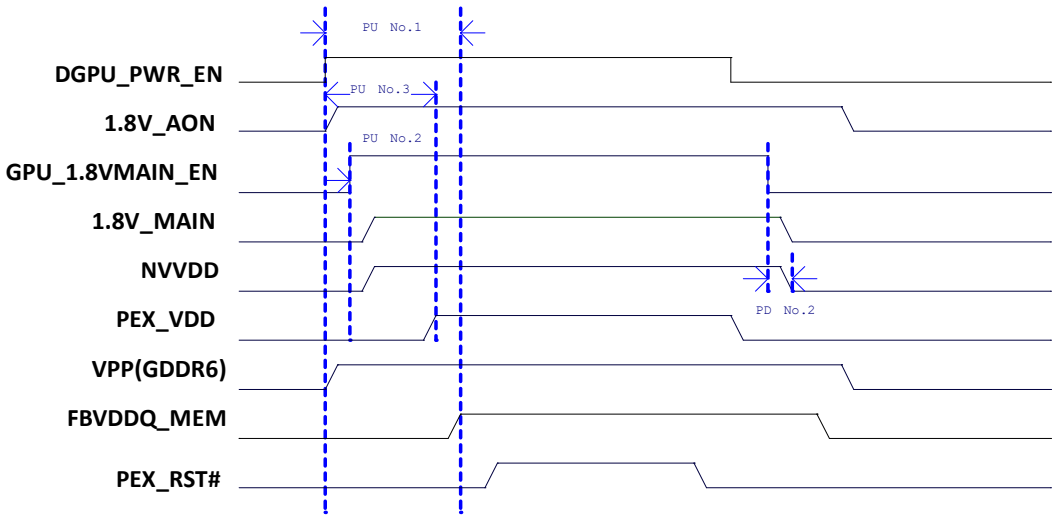


TGP Control	GPU_TGP_UP	OVRM_TGP_SEL
TGP Watt		
OVER 130W	High	High
100W to 110W	High	Low
115W to 130W (7S)	Low	High
75W to 90W (7Z)	Low	Low

dGPU	Thermal Design Power(TDP)			Output EDP - Continuous				Output EDPe Specification(is)		Output EDP-Peak(60s)			
	TGP(W)	GPU_TGP(W)	Memory_TGP(W)	VRDD(A)	FB Total(A)	1.0V Total(A)	1.5V Total(A)	VRDD(A)	FBVDD(A)	VRDD(A)	FB Total(A)	1.0V Total(A)	1.5V Total(A)
N18E-G1R MAX-Q	80(Baseline)	58	18	83	30	2.2	2.9	68	18	278	33	2.6	3.7
	85	62	18	86				72	18				
	90	67	18	96				75	18				
	105	72	19	106				84	18				
N18E-G2R MAX-Q	80(Baseline)	58	18	83	30	2.2	2.9	68	18	278	33	2.6	3.7
	85	62	18	90				72	18				
	90	67	18	96				75	18				
	105	72	19	106				84	18				
N18E-G3R MAX-Q	80(Baseline)	58	18	83	29	2.5	3	70	18	300	32	2.8	3.8
	85	62	18	90				74	18				
	90	67	18	97				78	18				
	105	76	19	110				87	18				
N18E-G1R	115	84	26	105	40	2.2	2.9	84	25	339	44	2.6	3.7
	115	84	26	105	40	2.2	2.9	84	25	339	44	2.6	3.7
N18E-G2R	150	118	20	151				119	21				
	160	126	20	150				125	21				
N18E-G3R	170	135	20	167	32	2.5	3	131	21	390	35	2.8	3.8
	180	143	20	174				138	21				
	190	152	20	180				144	21				
	200	160	20	181				150	21				

Comet Lake-H 8*2 45W		
CPU Power	100Max(A)	1PL1(A)
VCC	1.15	1.25
VCC_G7	32	25
VCC_SA	11.1	10

DGPU POWER SEQUENCE



POWER UP sequence is required:1.8V_AON->1.8V_MAIN->NVVDD->/PEX_DVDD->FBVDDQ_MEM

- 1.The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
- 2.Delay From GPU_1.8VMAIN_EN to PEX_DVDD/PG_PEX_VDD) must NOT exceed 4ms.
- 3.Delay From 1.8V_AON to PEX_DVDD/PG_PEX_VDD) must NOT exceed 20ms.
- 4.The ramp-up overshoot should not exceed the silicon reliability limit voltage
- 5.Power up NVVDD must be 90% before PEX_DVDD and NVVDDs can start ramp up.
- 6.Power up 1.8V_AON must be 90% before NV 3.3V ramp up.
- 7.All 3.3V devices that connect to the GPU must be powered after 1.8V_AON ; GPU can't have any 3.3V leakage path before 1.8V_AON present.
- 8.FBVDDQ.USB_VPP and 1.8_AON don't need power cycle for GC6

POWER DOWN sequence is required

- 1.PEX_DVDD must ramp down before NVVDD.
- 2.The propagation delay between GPU_1.8VMAIN_EN and the NVVDD EN pin needs to be less than 1ms during both power down.
- 3.For GDDR6,VPP must be equal to or higher than FBVDDQ at all time ; use gate logic and discharge circuit as needed.
- 4.All 3.3V devices that connect to the GPU must be ramp down before +1.8V_AON; GPU can't have any 3.3V leakage path after +1.8V_AON and +1.8V_MAIN power down.
- 5.Power down PEX_DVDD must be less than 10% before NVVDD can start ramp down.
- 6.Power down NV 3.3V must be less than 10% before +1.8V_AON can start ramp down.

